AT91CAP9-STK Starter Kit

User Guide

6351B–CAP–27-Jun-08

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Section 1

Introduction

1.1 Purpose

This document is a presentation of the hardware associated with the AT91CAP9-STK® Starter Kit.

This product is derived from the Atmel AT91CAP9-MZ and AT91CAP9-MB demonstration boards.

1.2 CAP™ Starter Kit Board

The AT91CAP9-STK Starter Kit is built on a single PCB, including:

- AT91CAP9S ARM926EJ-S™ -based microcontroller system-on-chip
- 64M Bytes of SDRAM application memory
- 512M Bytes of NAND Flash
- DataFlash® with up to 8M Bytes
- External interfaces for:
  - 10/100 Base-T Ethernet
  - USB Host and Full Speed/High Speed Device
  - ¼ VGA LCD Panel with Touch Screen
  - SD Card
  - 4 analog inputs
  - audio headphones
- Altera® Stratix®2 EP2S15F484 FPGA and its associated EPCS16 serial configuration memory. The FPGA provides 15600 four-input Lookup Table (LUT) equivalents, corresponding to approximately 124800 gates in the CAP MP Block.
- 64 general-purpose I/O connections from the AT91CAP9S, and 2 banks of 64 I/Os from the FPGA, for application-specific external interfaces
- CE-JTAG interface for CAP9 JTAG programming, and a USB-Blaster-JTAG interface for Stratix2 JTAG programming. These facilitate system debug.
- Atmel's AT73C224 and AT73C239 ICs for power supply and battery management.
- Atmel's AT73C213 for audio DAC
- Atmel's AT73C205 for battery charger

1.3 CAP Starter Kit Development Tools

The CAP Starter Kit is supplied with an essential set of development tools in order to get started immediately. These include:

- KickStart version of IAR™ Embedded Workbench® for ARM®
- Microsoft® Windows CE ® Board Support Package and demonstration from Adeneo
- Instructions for downloading Altera's free Quartus® 2 Web Edition tools for FPGA programming

1.4 Related Documents

1.4.1 Standards

JTAG IEEE® 1149.1 Standard.

1.4.2 Reference Documents

Table 1-1. Reference Documents

Description	Reference
Evaluation motherboard ORCAD schematics	20061027_11H20_AT91CAP9.dsn
Evaluation motherboard BOM	20061212_BOMASSY_ID2400_MOTHERBOARD.xls
Evaluation mezzanine board ORCAD schematics	20061122_09H00_AT91CAP9_MEZ.dsn
Evaluation mezzanine board BOM	20061207_ID2399_BOMASSY_MEZZANINE.xls
Atmel Specification	New Specification CAP9 Starter Kit
CAP9-STK hardware description.doc	ref. 4658D03
CAP9-STK ORCAD schematics	ref. ADEC101389001
CAP9-STK BOM	ref. ADEC101389003
CAP9-STK equipment plan	ref. ADEC101389EQ2

1.5 Glossary

BOM	Bill Of Materials
ICE	In-Circuit Emulator
JTAG	Joint Test Action Group
CAP	Customizable Microcontroller-based SoC Platform
CAP9-STK	CAP9 Starter Kit
FPGA	Field Programmable Gate Array
I/O	Input/Output
MCI	Multimedia Card Interface
MPB	Metal Programmable Block
MPIO	Metal Programmable I/O
NC	Not Connected
OHCI	Open Host Controller Interface
PLL	Phase Locked Loop
PMC	Power Management Circuit

Section 2

Requirements

2.1 General Description

The CAP9-STK's objective is to provide a rapid evaluation of the AT91CAP9 product and its derivatives. It does not allow a full emulation of a customized version of the CAP9, but is intended to familiarize the user with the customization concept and architecture of the CAP9.

It also demonstrates the operations of the analog companions provided by Atmel's AT73C family of products and the availability of the operating systems and software layers.

2.2 Interface and Function General Overview

AT91CAP9-STK interfaces and functions are as follows:

(Refer also to Figure 2-1 on page 2-3.)

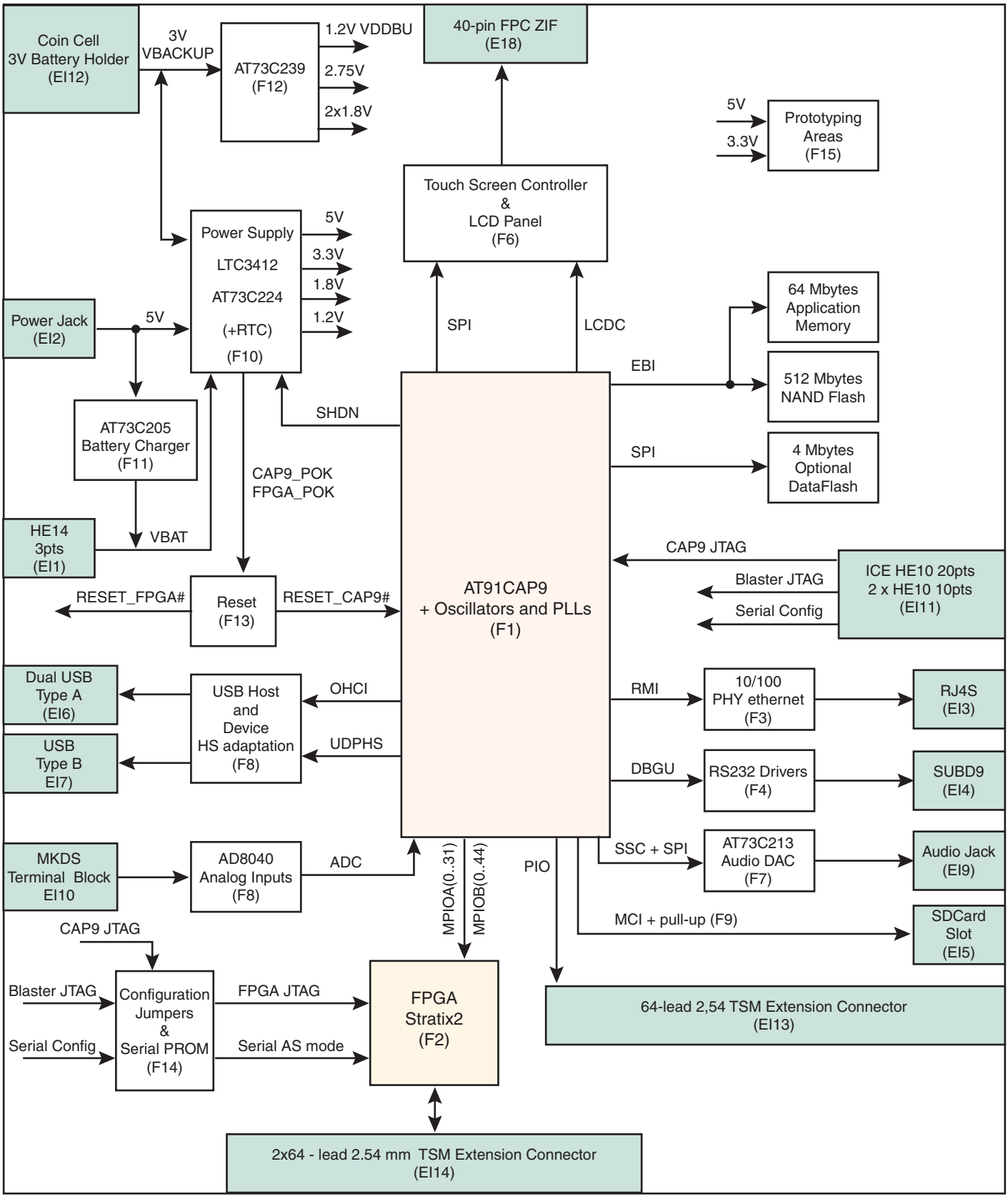
Interface

- EI1: 1 external Lithium-Ion battery
- EI2: 5V AC/DC sector adapter
- EI3: 1 RMII 10/100 Base-T Ethernet
- EI4: 1 Serial port, connected to the Debug Unit
- EI5: 1 SD Card slot
- EI6: 2 USB HOST interface
- EI7: 1 USB High Speed Device interface
- EI8: ¼ VGA LCD panel with Touch Screen
- EI9: 1 Audio stereo headset
- EI10: 4 Analog inputs
- EI11: 2 JTAG and 1 serial configuration interfaces
- EI12: 1 Manganese-Lithium coin battery
- EI13: 64-lead extension connector for the CAP9 I/O lines
- EI14: Two 64-lead extension connectors for the FPGA I/O lines

Function

- F1: AT91CAP9 microcontroller
- F2: FPGA and MPIO bus
- F3: RMII 10/100 Base-T Fast-Ethernet PHY Auto-MDIX.
- F4: RS232 driver
- F5: USB Host and Device
- F6: Touch screen controller and LCD panel
- F7: Audio DAC
- F8: Analog Inputs adaptation
- F9: SD Card
- F10: Power supplies and low power mode
- F11: Battery charger
- F12: RTC and Backup
- F13: Reset configuration
- F14: Programming and configuration
- F15: Prototyping Area

Figure 2-1. AT91CAP9-STK Interface and Function Overview



2.3 External Interfaces

2.3.1 EI1: External Lithium-ion Battery

The AT91CAP9-STK board implements one external Li-Ion battery 3-pin HE14 type connector..

Table 2-1. HE 14-3 Pinout

Pin	Signal Name	Description	Type	Level
1	VBAT	Battery power	I/O	4,5V
2	GND	Electrical ground	O	-
3	BAT_TS	Thermistor temperature sense	I	4,5V

2.3.2 EI2: 5VAC/DC Sector Adapter

CAP9-STK board implements one RAPC722 Switchcraft right angle miniature power jack with the following electrical characteristics:

- Contact resistance: 30 mΩ max
- Current carrying capability: 5A

2.3.3 EI3: RMII 10/100 Base-T Ethernet

An RJ45 8-pin Integrated Magnetics Connector is implement for the 10/100 Base-T Ethernet interface.

The connector integrates a 1 nF capacitor for HF shielding of the signal with chassis ground. (External connection between chassis and electrical ground is possible too.)

Table 2-2. RJ45-8 Pinout

Pin	Signal Name	Description	Type
1	TX+	Positive differential emission	O
2	TX-	Negative differential emission	O
3	RX+	Positive differential reception	I
6	RX-	Negative differential reception	I
4, 5, 7, 8	NC	-	-

2.3.4 EI4: Serial Port, Connected to the Debug Unit

A Debug right angle SUBD-9 connector is available in order to communicate with the AT91CAP9 microcontroller debug unit. This port is an electrical RS232 type connection. The connector integrates 2 additional pins (10, 11) for signal shielding.

Table 2-3. SUBD-P Pinout

Pin	Signal Name	Description	Type	Level
2	RXD	RS232 receive	I	±30V
3	TXD	RS232 transmit	O	±5V to ±5.2V
5, 10, 11	GND	Electrical ground	-	-
1, 4, 6, 7, 8, 9	NC	-	-	-

2.3.5 EI5: SD Card Slot

The AT91CAP9-STK board implements a 12-pin short type SDCARD slot on the bottom side.

Table 2-4. SD CARD Pinout

Pin	Signal Name	Description	Type	Level
1	MCI_DA3	Data 3	I/O	3.3V
2	MCI_CDA	Command/response	I/O open-drain	3.3V
3	GND	Electrical ground	-	-
4	3V3	3.3V power supply	O	3.3V
5	MCI_CK	Clock	O	3.3V
6	GND	Electrical ground	-	-
7	MCI_DA0	DATA 0	I/O	3.3V
8	MCI_DA1	DATA 1	I/O	3.3V
9	MCI_DA2	DATA 2	I/O	3.3V
10	MCI_CD	Card Detect	I	3.3V
11	GND	Electrical ground	-	-
12	NC	-	-	-

2.3.6 EI6: Two USB Host Interfaces

Two USB HOST connectors are available on a sign dual-port Type A connector.

Table 2-5. Dual-port Type A Connector Pinout

Pin	Signal Name	Description	Type
A1	5V	5V power supply (fuse 500mA)	O
A2	HDMA	Negative differential port A	I/O
A3	HDPA	Positive differential port A	I/O
A4	GND	Electrical ground	-
B1	5V	5V power supply (fuse 500mA)	O
B2	HDMB	Negative differential port B	I/O
B3	HDPB	Positive differential port B	I/O
B4	GND	Electrical ground	-
1 to 4	GND	Electrical ground	-

2.3.7 EI7: USB High Speed Device Interface

One USB Device High/Full Speed connector is available on a Type B connector.

Table 2-6. Type B Connector Pinout

Pin	Signal Name	Description	Type	Level
1	VBUS	5V supply	I	1
2	HSDM / FSDM	Negative differential port A	I/O	2
3	HSDP / FSDP	Positive differential port A	I/O	3
4, 5, 6	GND	Electrical	-	4, 5, 6

2.3.8 EI8: 1/4 VGA LCD Panel with Touch Screen

The AT91CAP9-STK board implements a 0.5 FPC, 40-pin ZIF LCD Panel connector, with contact on the bottom side. The connector integrates two additional pins (MC1, MC2) for signal shielding.

Table 2-7. 40-pin ZIF Connector Pinout

Pin	Signal Name	Description	Type	Level
1	3V3	3.3V power supply	O	3.3V
2	3V3	3.3V power supply	O	3.3V
3	3V3	3.3V power supply	O	3.3V
4	LCDDOTCK	Dot clock	O	3.3V
5	GND	Electrical ground	-	-
6	LCDHSYNC	Horizontal synchronization pulse	O	3.3V
7	GND	Electrical ground	-	-
8	LCDDEN	Timing signal for data	O	3.3V
9	GND	Electrical ground	-	-
10	NC	-	-	-
11	GND	Electrical ground	-	-
12	LCDD7	RED data 5	O	3.3V
13	LCDD6	RED data 4	O	3.3V
14	LCDD5	RED data 3	O	3.3V
15	GND	Electrical ground	-	-
16	LCDD4	RED data 2	O	3.3V
17	LCDD3	RED data 1	O	3.3V
18	LCDD2	RED data 0	O	3.3V
19	GND	Electrical ground	-	-
20	LCDD15	GREEN data 5	O	3.3V
21	LCDD14	GREEN data 4	O	3.3V
22	LCDD13	GREEN data 3	O	3.3V
23	GND	Electrical ground	-	-
24	LCDD12	GREEN data 2	O	3.3V
25	LCDD11	GREEN data 1	O	3.3V
26	LCDD10	GREEN data 0	O	3.3V
27	GND	Electrical ground	-	-
28	LCDD23	BLUE data 5	O	3.3V
29	LCDD22	BLUE data 4	O	3.3V
30	LCDD21	BLUE data 3	O	3.3V
31	GND	Electrical ground	-	-
32	LCDD20	BLUE data 2	O	3.3V
33	LCDD19	BLUE data 1	O	3.3V
34	LCDD18	BLUE data 0	O	3.3V
35	PCI	Power control	O	3.3V

Table 2-7. 40-pin ZIF Connector Pinout (Continued)

Pin	Signal Name	Description	Type	Level
36	VCTRL	LED current control	O	3.3V
37	Y_UP	Touch panel upper side	O	3.3V
38	X_LEFT	Touch panel left side	O	3.3V
39	Y_LOW	Touch panel low side	O	3.3V
40	X_RIGHT	Touch panel right side	O	3.3V

2.3.9 EI9: Audio Stereo Headset

A headset audio interface connector is available for a 3.5 phone jack stereo plug.

SMT 1503-03 Lumberg is used.

2.3.10 EI10: Analog Inputs

The AT91CAP9-STK board implements a 3.81mm-pitch Phoenix MKDS 6-pin terminal block. This connector receives four analog inputs.

Table 2-8. MKDS 6-pin Terminal Block Pinout

Pin	Signal Name	Description	Type	Level
1	ANALOG_I1	Analog input 1	I	3.3V
2	ANALOG_I2	Analog input 2	I	3.3V
3	ANALOG_I3	Analog input 3	I	3.3V
4	ANALOG_I4	Analog input 4	I	3.3V
5	GND	Electrical ground	-	-
6	NC (3V3)	- (It can be connected to 3.3V by 0Ω strap)	- (O)	- (3.3V)

2.3.11 EI11: JTAG and Serial Configuration Interfaces

Two programming JTAG interfaces and one serial configuration device interface are available on the board.

2.3.11.1 ICE-JTAG Interface

One ICE-JTAG interface is a right angle male, HE10 2x10-pin connector, to receive CAP9 ICE debugger probe for CAP9 JTAG programming.

Table 2-9. HE10 2x10-pin Connector Pinout

Pin	Signal Name	Description	Type	Level
1	3V3	3.3V power supply	O	3.3V
3	NTRST	Test Reset	I	3.3V (active low)
5	TDI	Test Data In	I	3.3V
7	TMS	Test Mode Select	I	3.3V
9	TCK	Test Clock	I	3.3V
11	RTCK	Returned Test Clock	O	3.3V
13	TDO	Test Data Out	O	3.3V

Table 2-9. HE10 2x10-pin Connector Pinout (Continued)

Pin	Signal Name	Description	Type	Level
15	NRST	Microcontroller Reset	I/O	3.3V (active low)
17, 19	NC	-	-	-
4, 6, 8, 10, 12, 14, 16, 18, 20	GND	Electrical ground	-	-

2.3.11.2 USB-Blaster-JTAG Interface

One USB-Blaster-JTAG interface is a straight male, HE10 2x5-pin connector, to receive the Altera FPGA USB Blaster probe for Stratix2 JTAG programming.

Table 2-10. HE10 2x5-pin Connector Pinout

Pin	Signal Name	Description	Type	Level
1	TCK	Test Clock	I	3.3V
3	TDO	Test Data Out	O	3.3V
5	TMS	Test Mode Select	I	3.3V
9	TDI	Test Data In	I	3.3V
4, 6	3V3	3.3V power supply	O	3.3V
7, 8	NC	-	-	-
2, 10	GND	Electrical ground	-	-

2.3.11.3 Serial Configuration Device Interface

The serial configuration device interface is a straight male, HE10 2x5-pin connector, to receive the Altera FPGA USB Blaster probe for serial EPCS Device programming.

Table 2-11. HE10 2x5-pin Connector Pinout

Pin	Signal Name	Description	Type	Level
1	DCLK	Configuration Clock pin	O	3.3V
3	CONF_DONE	Configuration Status pin	I/O	3.3V open-drain
5	nCONFIG	Configuration Control input	I	3.3V
6	nCE	Configuration Chip enable	I	3.3V (active low)
7	DATA0	Configuration Data input	I	3.3V
8	nCSO	Configuration Chip select	O	3.3V
9	ASDO_FPGA	Configuration Read enable	O	3.3V
4	3V3	3.3V power supply	O	3.3V
2, 10	GND	Electrical ground	-	-

2.3.12 EI12: Manganese-Lithium Coin Battery

The AT91CAP9-STK board implements a coin cell battery holder for 12 mm rechargeable 3V Manganese-Lithium coin battery, Panasonic ML1220 type.

3V non-rechargeable Lithium coin batteries are not supported.

2.3.13 EI13: 64-lead Extension Connector for the AT91CAP9 I/O Lines

A straight male, 2.54 mm-pitch, 64-pin connector is available on the board as a CAP9 extension connector.

Table 2-12. 64-pin Connector Pinout

Pin	Signal Name	Level	Pin	Signal Name	Level
1	5V	5V	2	5V	5V
3	5V	5V	4	GND	-
5	GND	-	6	GND	-
7	3V3	3.3V	8	3V3	3.3V
9	PA2/SPI0_SPCK	3.3V	10	GND	-
11	GND	-	12	PA0/SPI0_MISO	3.3V
13	PA9	3.3V	14	GND	-
15	GND	-	16	PA1/SPI0_MOSI	3.3V
17	PD1/SPI0_NPCS3	3.3V	18	PD0	3.3V
19	GND	-	20	3V3	3.3V
21	TWCK	3.3V open-drain	22	PA10/IRQ0	3.3V
23	GND	-	24	PA14/IRQ1	3.3V
25	TWD	3.3V open-drain	26	PA22/TXD0	VDDIOP1
27	PA24/RTS0	VDDIOP1	28	PA23/ RXD0	VDDIOP1
29	GND	-	30	PB12/SPI1_MISO	3.3V
31	PA27/PCK1	VDDIOP1	32	PB13/SPI1_MOSI	3.3V
33	VDDIOP1	3.3V or 1.8V	34	GND	-
35	PA26	VDDIOP1	36	PB14/SPI1_SPCK	3.3V
37	PA29	VDDIOP1	38	GND	-
39	PA30	VDDIOP1	40	PB15/SPI1_NPCS0	3.3V
41	PA31	VDDIOP1	42	PB16/SPI1_NPCS1	3.3V
43	VDDIOP1	3.3V or 1.8V	44	3V3	3.3V
45	GND	-	46	3V3	3.3V
47	PC12	3.3V	48	PC29	3.3V
49	PC13	3.3V	50	GND	-
51	PD2	3.3V	52	PD5/DMARQ2	3.3V
53	PC3	3.3V	54	GND	-
55	GND	-	56	PD6/NWAIT	1.8V
57	PD8/NCS5	1.8V	58	PD7/NCS4	1.8V
59	PD10/SCK1	1.8V	60	PD9/SCK2	1.8V
61	PD13/A24	1.8V	62	PD12/A23	1.8V
63	PD14 / A25	1.8V	64	1V8_CAP9	1,8V

2.3.14 EI14: Two 64-lead Extension Connectors for the FPGA I/O Lines

Two straight male, 2.54 mm-pitch, 64-pin connectors are available on the board as FPGA extension connectors.

The pinouts for both FPGA connectors are given in Table 2-13 and Table 2-14

Table 2-13. 64-pin Connector Pinout and Bank Assignment

Pin	FPGA IO/Power Name	Bank	Pin	FPGA IO/Power Name	Bank
1	GND	-	2	VCCIO4	BANK4
3	FPGA_IO0	BANK4	4	VCCIO4	BANK4
5	FPGA_IO1	BANK4	6	FPGA_IO2	BANK4
7	FPGA_IO3	BANK4	8	FPGA_IO4	BANK4
9	FPGA_IO5	BANK4	10	GND	-
11	FPGA_IO6	BANK4	12	FPGA_IO7	BANK4
13	FPGA_IO8	BANK4	14	FPGA_IO9	BANK4
15	FPGA_IO10	BANK4	16	FPGA_IO11	BANK4
17	FPGA_IO12	BANK4	18	FPGA_IO13	BANK4
19	GND	-	20	FPGA_IO14	BANK4
21	FPGA_IO15	BANK4	22	FPGA_IO16	BANK4
23	FPGA_IO17	BANK4	24	FPGA_IO18	BANK4
25	FPGA_IO19	BANK4	26	FPGA_IO20	BANK4
27	FPGA_IO21	BANK4	28	GND	-
29	FPGA_IO22	BANK4	30	FPGA_IO23	BANK4
31	FPGA_IO24	BANK4	32	FPGA_IO25	BANK4
33	FPGA_IO26	BANK4	34	FPGA_IO27	BANK4
35	GND	-	36	FPGA_IO28	BANK6
37	FPGA_IO29	BANK6	38	FPGA_IO30	BANK6
39	FPGA_IO31	BANK6	40	FPGA_IO32	BANK6
41	FPGA_IO33	BANK6	42	FPGA_IO34	BANK6
43	FPGA_IO35	BANK6	44	FPGA_IO36	BANK6
45	FPGA_IO37	BANK6	46	GND	-
47	FPGA_IO38	BANK6	48	FPGA_IO39	BANK6
49	FPGA_IO40	BANK6	50	FPGA_IO41	BANK6
51	FPGA_IO42	BANK6	52	FPGA_IO43	BANK6
53	FPGA_IO44	BANK6	54	FPGA_IO45	BANK6
55	GND	-	56	FPGA_IO46	BANK6
57	FPGA_IO47	BANK6	58	FPGA_IO48	BANK6
59	FPGA_IO49	BANK6	60	FPGA_IO50	BANK6
61	VCCIO6	BANK6	62	FPGA_IO51	BANK6
63	VCCIO6	BANK6	64	GND	-

Table 2-14. 64-pin Connector Pinout and Bank Assignment

Pin	FPGA IO/Power Name	Bank	Pin	FPGA IO/Power Name	Bank
1	GND	-	2	VCCIO6	BANK6
3	FPGA_IO	BANK6	4	VCCIO6	BANK6
5	FPGA_IO	BANK6	6	FPGA_IO	BANK6
7	FPGA_IO	BANK6	8	FPGA_IO	BANK6
9	FPGA_IO	BANK6	10	GND	-
11	FPGA_IO	BANK7	12	FPGA_IO	BANK7
13	FPGA_IO	BANK7	14	FPGA_IO	BANK7
15	FPGA_IO	BANK7	16	FPGA_IO	BANK7
17	FPGA_IO	BANK7	18	FPGA_IO	BANK7
19	GND	-	20	FPGA_IO	BANK7
21	FPGA_IO	BANK7	22	VCCIO7	BANK7
23	FPGA_IO	BANK7	24	VCCIO7	BANK7
25	FPGA_IO	BANK7	26	FPGA_IO	BANK7
27	FPGA_IO	BANK7	28	GND	-
29	FPGA_IO	BANK7	30	FPGA_IO	BANK7
31	FPGA_IO	BANK7	32	FPGA_IO	BANK7
33	FPGA_IO	BANK7	34	FPGA_IO	BANK7
35	FPGA_IO	BANK7	36	FPGA_IO	BANK7
37	GND	-	38	FPGA_IO	BANK7
39	FPGA_IO	BANK7	40	FPGA_IO	BANK7
41	FPGA_IO	BANK7	42	FPGA_IO	BANK7
43	VCCIO8	BANK8	44	FPGA_IO	BANK7
45	VCCIO8	BANK8	46	GND	-
47	FPGA_IO	BANK8	48	FPGA_IO	BANK8
49	FPGA_IO	BANK8	50	FPGA_IO	BANK8
51	FPGA_IO	BANK8	52	FPGA_IO	BANK8
53	FPGA_IO	BANK8	54	FPGA_IO	BANK8
55	GND	-	56	FPGA_IO	BANK8
57	FPGA_PLLOUTp	3.3V	58	GND	-
59	GND	-	60	FPGA_IO	BANK8
61	FPGA_PLLOUTn	3.3V	62	GND	-
63	GND	-	64	3V3	3.3V

2.4 Characteristics

2.4.1 Functional Characteristics

2.4.1.1 F1: AT91CAP9 Microcontroller

The AT91CAP9-STK microcontroller core block implements the necessary digital-system core functions.

It's composed of the following elements:

- One 32-bit-ARM9® AT91CAP9 microcontroller core and its power supplies (see below).
- One 1.8V, 512 Mbytes, 8-bit NAND Flash,
- One 1.8V, 64 Mbytes, 32-bit SDRAM Application Volatile Memory
- One optional 3.3V DataFlash® memory from 512 Kbytes to 8 Mbytes
- One Debug and JTAG Test unit (See “F14: Programming and Configuration” on page 2-27.)
- One MPB

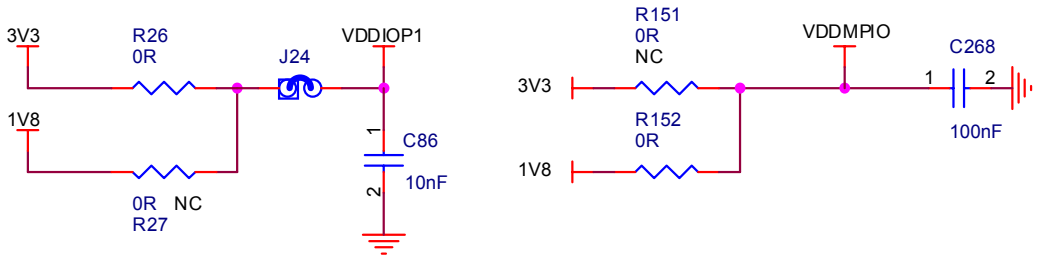
2.4.1.1.1 AT91CAP9 Power Supplies

The power supply of the AT91CAP9 Microcontroller is shown below.

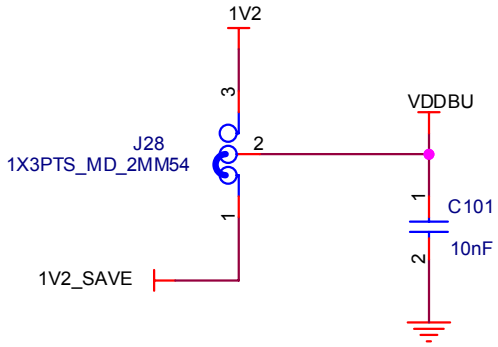
Table 2-15. AT91CAP9 Power Supply

Power Supply Name	Power Supply
VDDCORE	1V2_CAP9
VDDPLL	3V3
VDDUPLL	1V2_CAP9 (RC filtered)
VDDUTMII	3V3
VDDIOP0	3V3
VDDIOP1	3V3 or 1V8_CAP9
VDDUTMIC	1V2_CAP9
VDDIOM	1V8
VDDMPIO	3V3 or 1V8_FPGA
VDDBU	1V2_SAVE or 1V2_CAP9
VDDANA	3V3 filtered
VREFP	VREFP (3V)

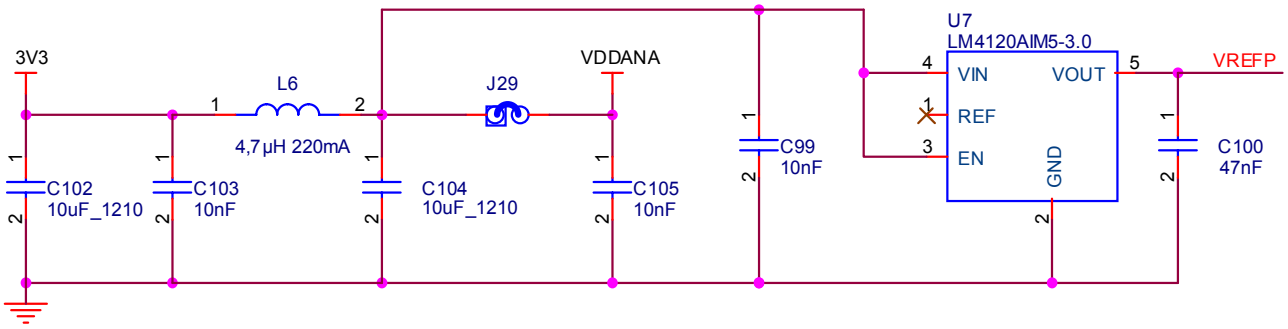
- For VDDIOP1 and VDDMPI0, the choice is made by 0Ω resistors:



- For VDDBU, the choice is made by a jumper on the 3-pin J28 connector:



- The implementation of VDDANA and VREEP is shown below.



2.4.1.1.2 AT91CAP9 Clocks

The internal clocks of the AT91CAP9 are generated by two external quartz sources:

- 12 Mhz quartz for the MAINCK internal clock
- 32,768 kHz quartz for the SLCK internal slow clock

2.4.1.2 F2: FPGA and MPIO Bus

2.4.1.2.1 FPGA Characteristics

This function is performed by an Altera Stratix2, EP2S15F484 FPGA and its EPCS16 serial configuration device.

Stratix2 EP2S,15F484 FPGA characteristics are:

- 15600 equivalent LE (LE is four-input LUT-based architecture),
- 1.2V core power supply, 3.3V or 1.8V I/O bank power supplies,
- 484-pin FBGA,
- -5 speed grade.

The FPGA aims to emulate the logic to be implemented in the MPB through 5 metal layers.

The FPGA also manages the EI14 interface.

2.4.1.2.2 MPIO Bus Characteristics

The FPGA is connected to the AT91CAP9 microcontroller through the two MPIO buses:

- First MPIO bus: MPIOA[0:31], connected to FPGA bank 1
- Second MPIO bus: MPIOB[0:44], connected to FPGA banks 2 and 5
- Bus frequency: 100MHz
- Dedicated MPIO bus clock: MPIOB24

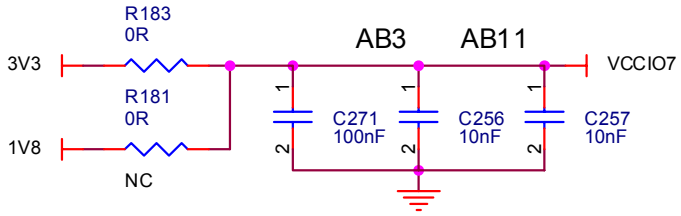
2.4.1.2.3 FPGA Power Supplies

Table 2-16. FPGA Bank Power Supplies

Bank 1	VDDMPIO (default 1V8_FPGA)
Bank 2	VDDMPIO (default 1V8_FPGA)
Bank 3	3V3
Bank 4	VCCIO4 (default 3V3)
Bank 5	VDDMPIO (default 1V8_FPGA)
Bank 6	VCCIO6 (default 1V8_FPGA)
Bank 7	VCCIO7 (default 3V3)
Bank 8	VCCIO8 (default 3V3)
Bank 9	3V3
Bank 10	3V3

Power for VDDMPIO, VCCIO4, VCCIO6, VCCIO7, and VCCIO8 can be supplied either by 3V3 or 1V8 (1V8_CAP9) power supplies. (See “F10: Power Supplies and Low-power Mode” on page 2-22.)

Choice is made by 0Ω resistor as shown below (VCCIO7 example):



Each of the six FPGA PLL blocks have two power supply pins: VCCA_PPLw and VCCD_PPLx (x = from to 6).

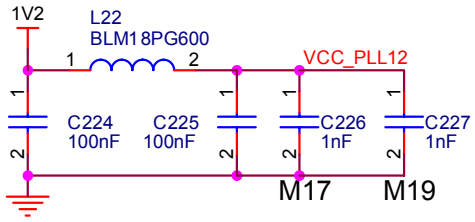
Table 2-17. FPGA PLL Block Power Supply

PLL Supply Pin Name	Power Supply
VCCA_PPL1	VCC_PLL12
VCCA_PPL2	VCC_PLL12
VCCA_PPL3	VCC_PLL34
VCCA_PPL4	VCC_PLL34
VCCA_PPL5	VCC_PLL56

Table 2-17. FPGA PLL Block Power Supply (Continued)

PLL Supply Pin Name	Power Supply
VCCA_PPL6	VCC_PLL56
VCCD_PPL1	1V2_CAP9
VCCD_PPL2	1V2_CAP9
VCCD_PPL3	1V2_CAP9
VCCD_PPL4	1V2_CAP9
VCCD_PPL5	1V2_CAP9
VCCD_PPL6	1V2_CAP9

VCC_PLL12, VCC_PLL34, VCC_PLL56 are 1V2 (1V2_CAP9) ferrite isolated power supplies as shown below (VCC_PLL12 example):

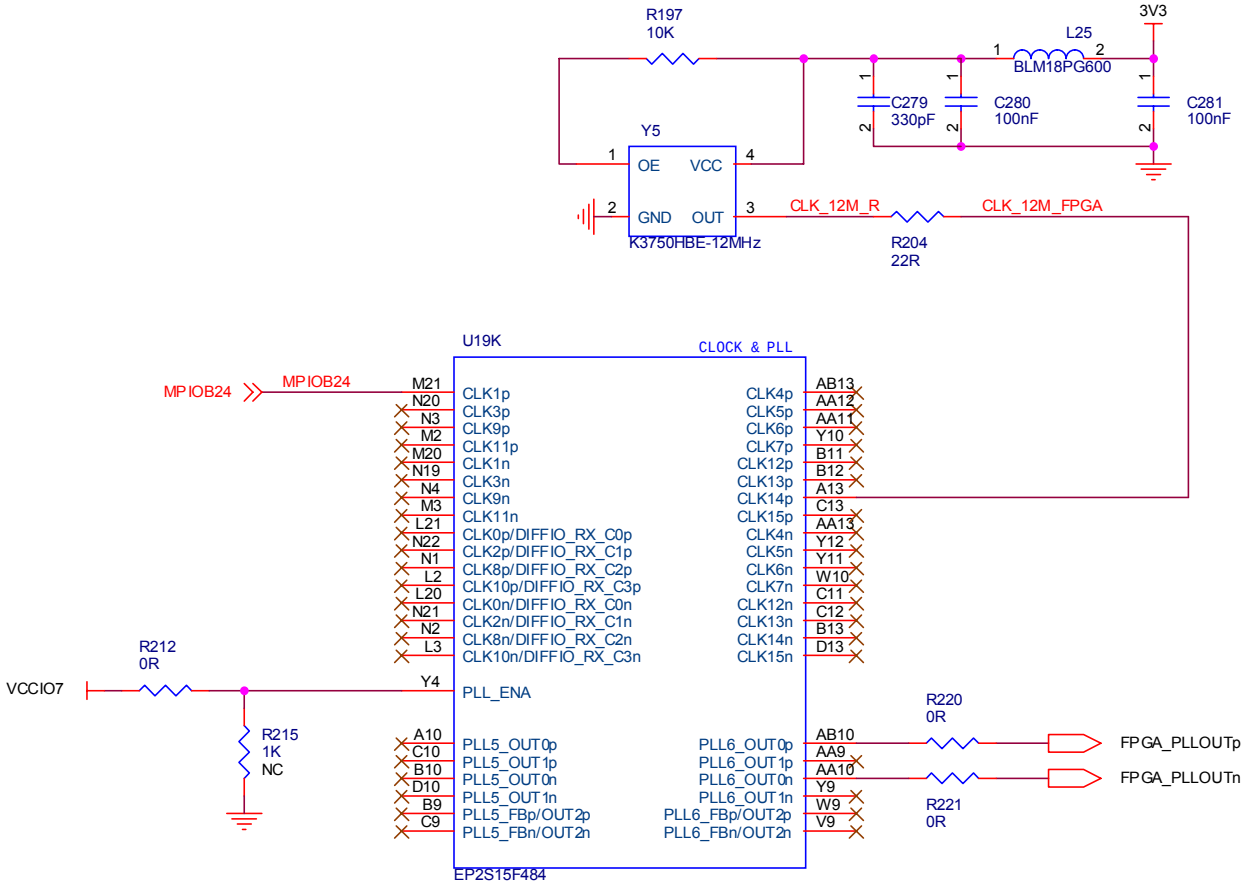


2.4.1.2.4 FPGA Clock

The MPIO Bus clock MPIOB24 is connected to the CLK1p clock input pin of the FPGA. An additional external 12 MHz oscillator generates clock to the CLK14p clock input pin of the FPGA.

Spare clock PLL_OUTp and PLL_OUTn are connected to the EI14 interface.

FPGA clock part electrical connection is shown below.

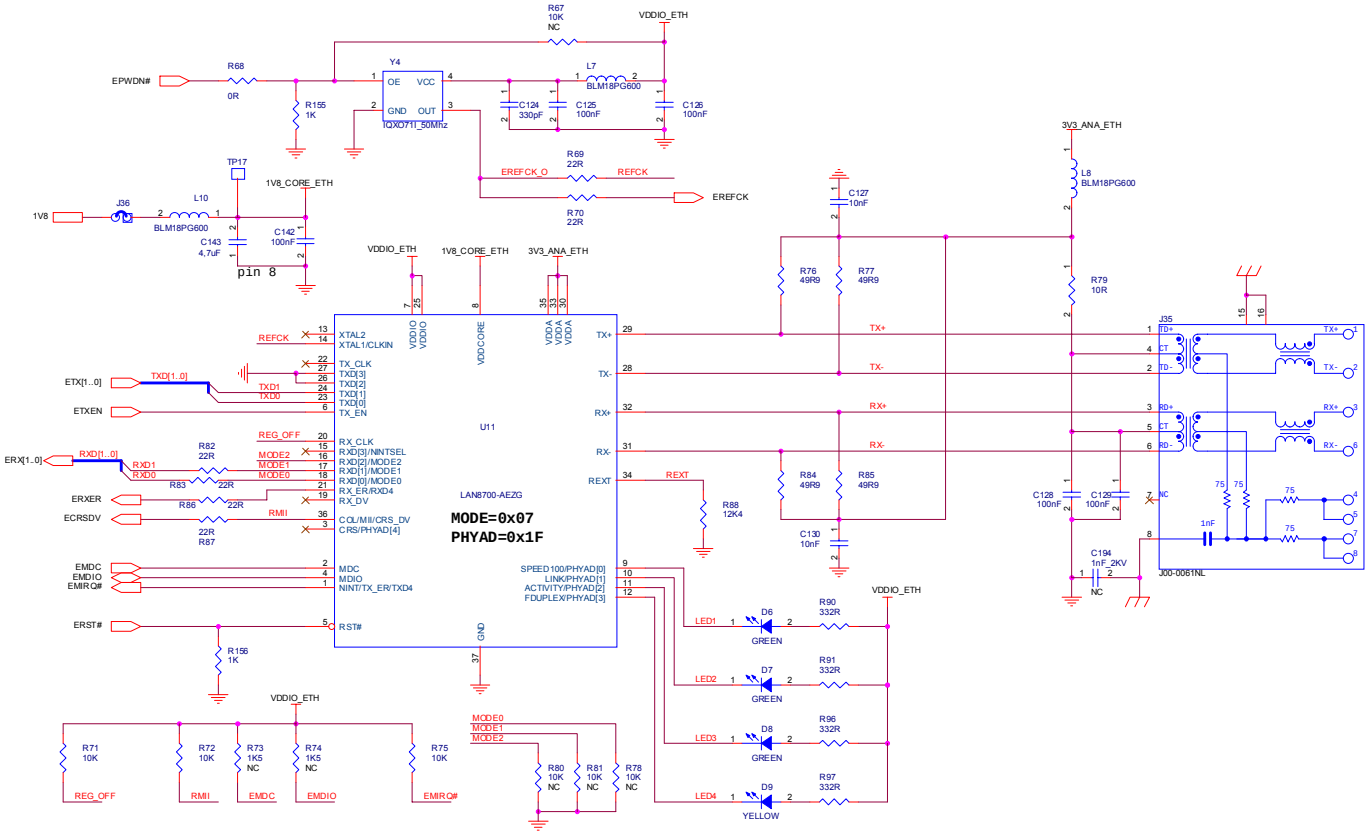


2.4.1.3 F3: RMII 10/100 Base-T Fast-Ethernet PHY Auto-MDIX

The 10/100 Ethernet MAC function is implemented in the AT91CAP9 EMAC module.

This module manages an RMII 10/100 Base-T Fast-Ethernet PHY Auto-MDIX (SMSC LAN8700) to implement a 10/100 Base-T Ethernet port.

The implementation is shown below.



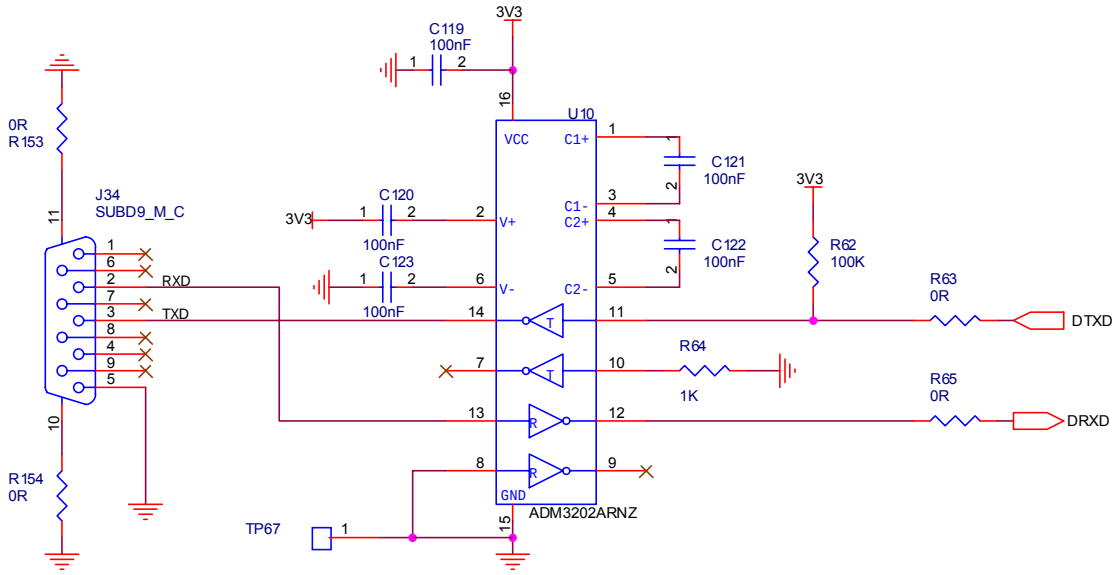
The 1.8V core power supply is external by default, to minimize 3.3V power consumption.

Use of LAN8700 3.3V/1.8V internal regulator can be done by disconnected J36 and R71 REG_OFF Pull-up.

2.4.1.4 F4: RS232 Driver

An ADM3202 RS232 driver is implemented for signal adaptation between RS232 signals (RXD, TXD) on the debug port connector and AT91CAP9 Debug unit 3.3V signals (DRXD, DTXD).

The implementation is shown below:



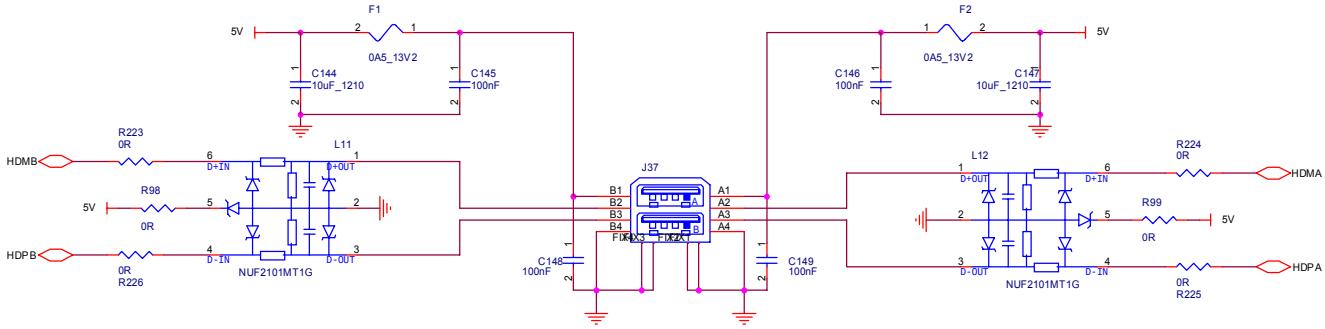
2.4.1.5 F5: USB Host and Device

2.4.1.5.1 USB Host

The two USB v2.0 Host interfaces are managed by the AT91CAP9 USB Host port, which handles OHCI protocol as well as USB v2.0 Full-speed and Low-speed protocols.

Two NUF2101 USB filters are implemented for ESD protection and line adaptation (26.3Ω to 33.7Ω). One 0603 footprint is implemented on each signal to adjust 39Ω line impedance if necessary.

One 500 mA SMD fuse is added on 5V power supply of each port.

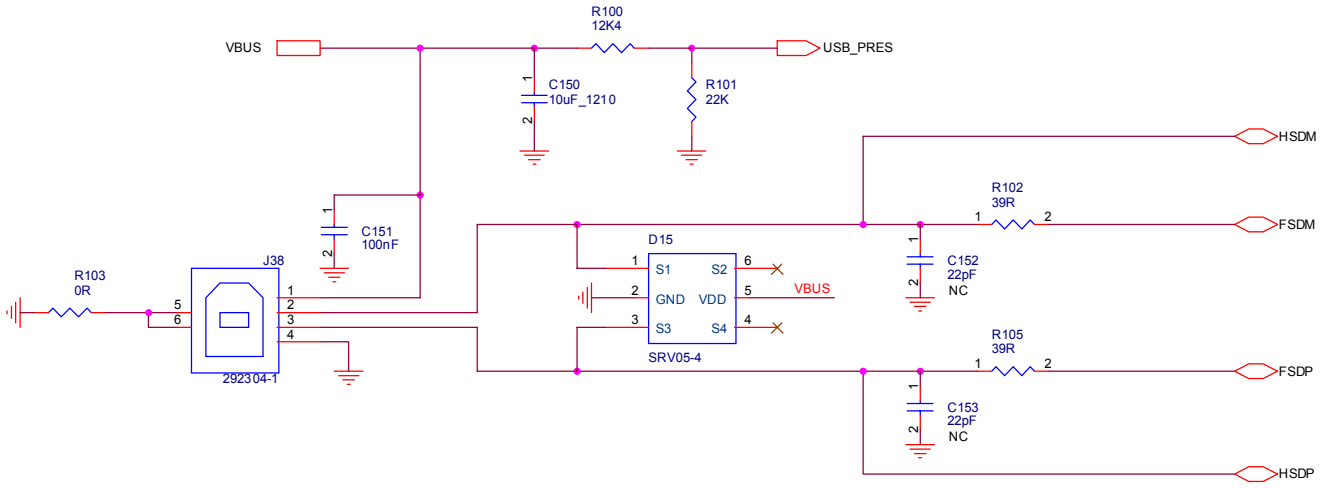


2.4.1.5.2 USB High Speed Device

The USB v2.0 High Speed Device interface is managed by the AT91CAP9 USB High Speed Device port compliant with the USB rev 2.0 High Speed device specification.

The necessary 1.5kΩ Pull-up to 3.3V on HSDP (and FSDP) is included in the AT91CAP9 USB device port.

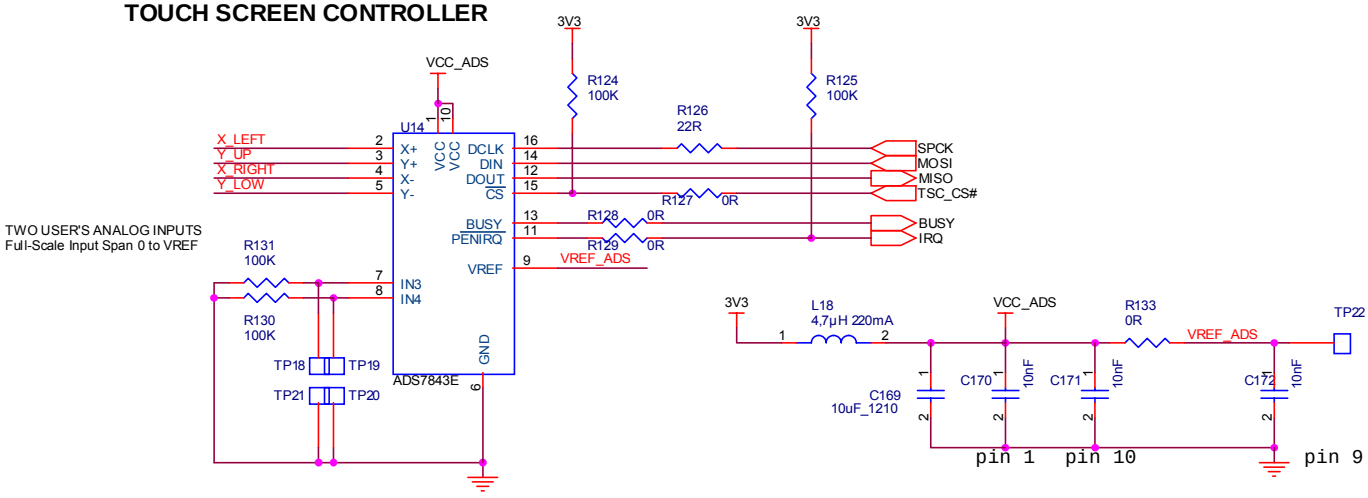
The implementation is shown below:



2.4.1.6 F6: Touch Screen Controller and LCD Panel

An ADS7843E touch screen controller is implemented on the board. It's controlled by the AT91CAP9 SPI0 bus, with SPI0_NPCS1 chip select.

The figure below, derived from the AT91SAM9261-EK schematics, shows the implementation:

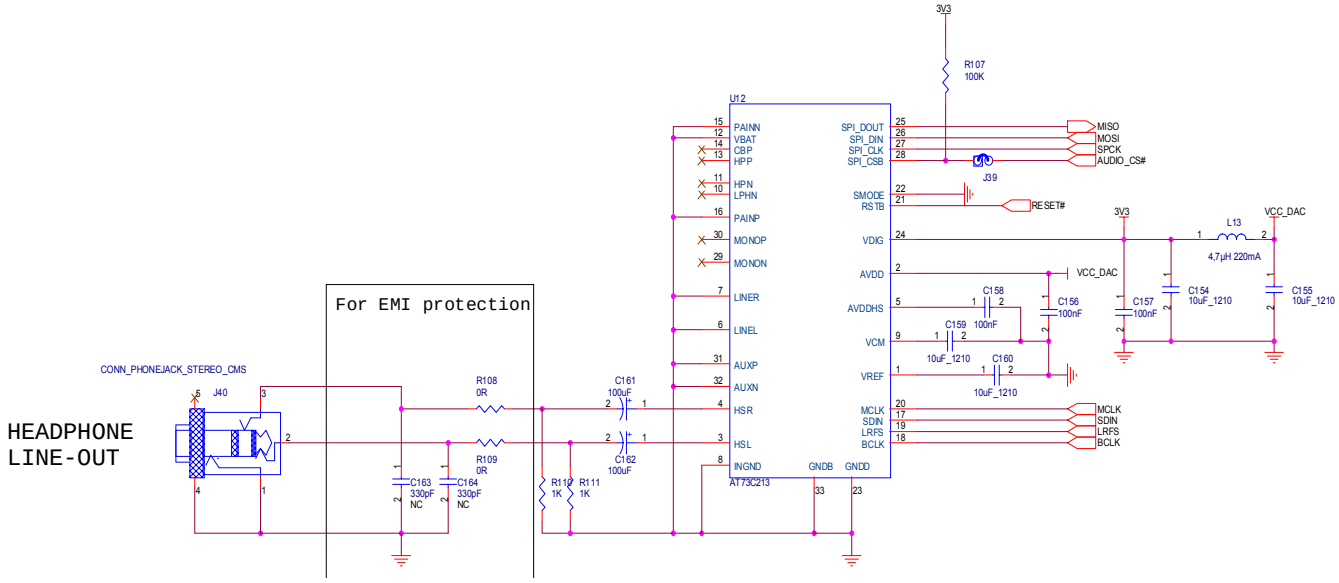


The LCD panel controlled the AT91CAP9 LCD Controller.

2.4.1.7 F7: Audio DAC

The AT73C213 DAC is used for the I²S audio output. It's controlled by the AT91CAP9 SPI0 bus, with SPI0_NPCS2 chip select. I²S DAC dedicated serial interface is managed by AT91CAP9 SCC0 bus.

The implementation is shown below:



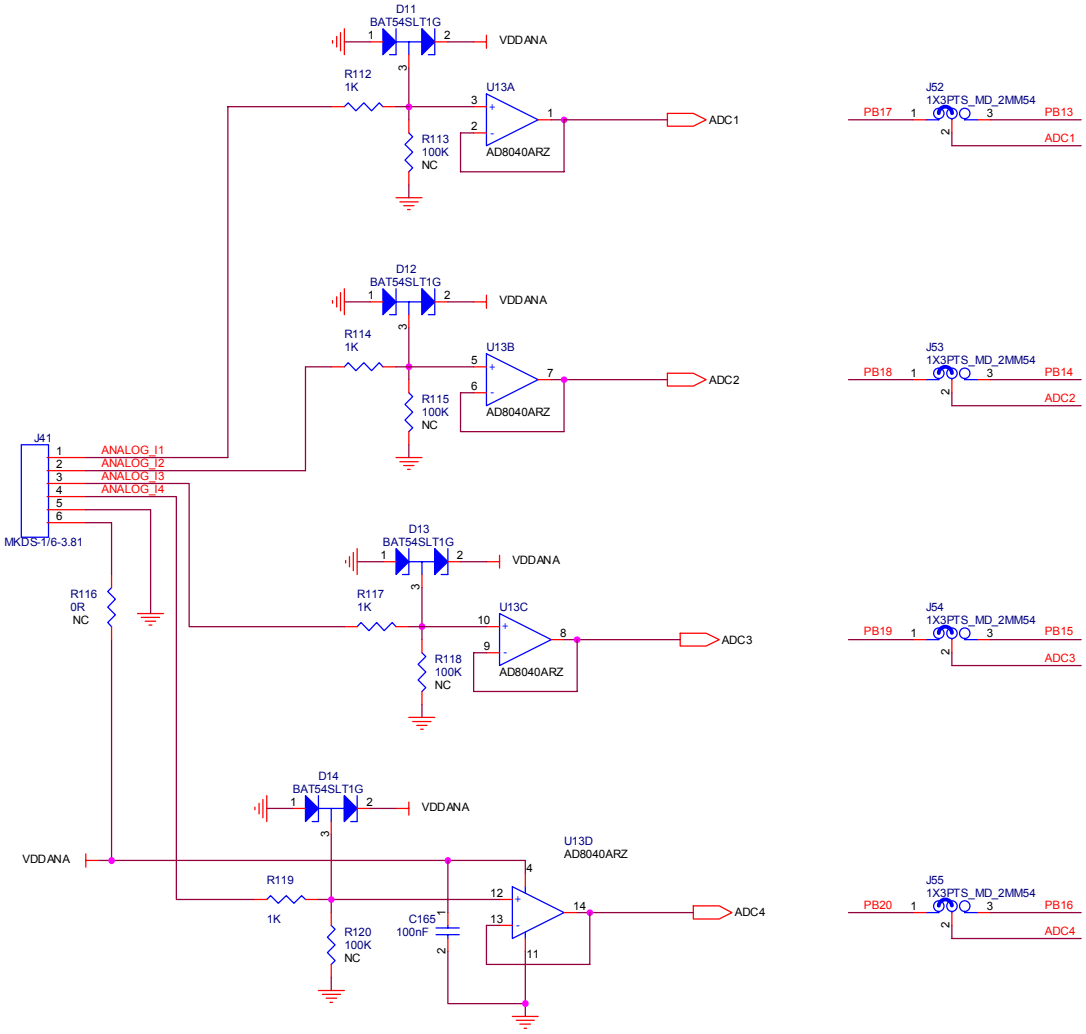
2.4.1.8 F8:Analog Input Adaptation

Analog input adaptation is realized by an AD8040 low-power high-speed rail-to-rail IO amplifier. ADC[1..4] output signals of the amplifier drive the AD[0..7] ADC embedded in the AT91CAP9.

Table 2-18.

Analog Signal Name	J52 jumper Position	J53 jumper Position	J54 jumper Position	J55 jumper Position	AT91CAP9 ADC Name
ADC1	1-2 (default)	-	-	-	AD4
ADC1	2-3	-	-	-	AD0
ADC2	-	1-2 (default)	-	-	AD5
ADC2	-	2-3	-	-	AD1
ADC3	-	-	1-2 (default)	-	AD6
ADC3	-	-	2-3	-	AD2
ADC4	-	-	-	1-2 (default)	AD7
ADC4	-	-	-	2-3	AD3

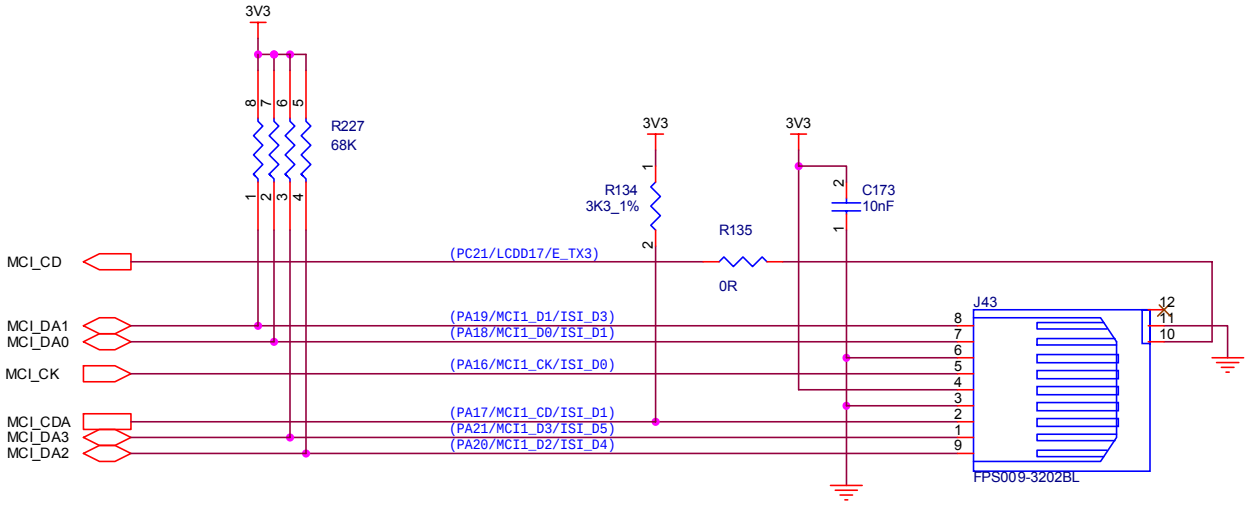
The implementation is shown below


D11
BAT54SLT1G
VDDANA
R112
1K
U13A
R113
100K
NC
AD8040ARZ
ADC1
J52
1X3PTS_MD_2MM54
PB17
PB13
ADC1
D12
BAT54SLT1G
VDDANA
R114
1K
U13B
R115
100K
NC
AD8040ARZ
ADC2
J53
1X3PTS_MD_2MM54
PB18
PB14
ADC2
J41
ANALOG_I1
ANALOG_I2
ANALOG_I3
ANALOG_I4
MKDS-1/6-3.81
D13
BAT54SLT1G
VDDANA
R116
0R
NC
R117
1K
U13C
R118
100K
NC
AD8040ARZ
ADC3
J54
1X3PTS_MD_2MM54
PB19
PB15
ADC3
D14
BAT54SLT1G
VDDANA
VDDANA
U13D
AD8040ARZ
R119
1K
R120
100K
NC
C165
100nF
ADC4
J55
1X3PTS_MD_2MM54
PB20
PB16
ADC4

2.4.1.9 F9: SD Card

The AT91CAP9 MCI is directly connected to the SD Card slot. 68k pull-up resistors are added on the MCI_DA[0..3] data signals.

The implementation is shown below:

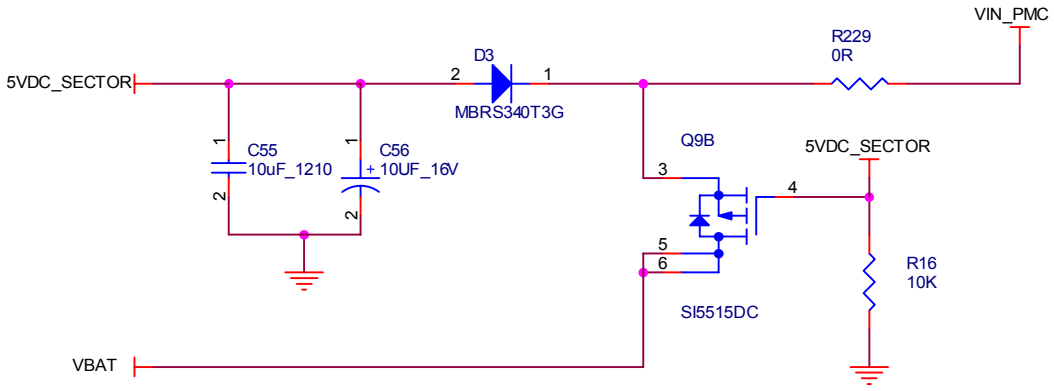


2.4.1.10 F10: Power Supplies and Low-power Mode

0603 footprint (0Ω resistor) or jumpers are implemented on power supplies in order to measure the current.

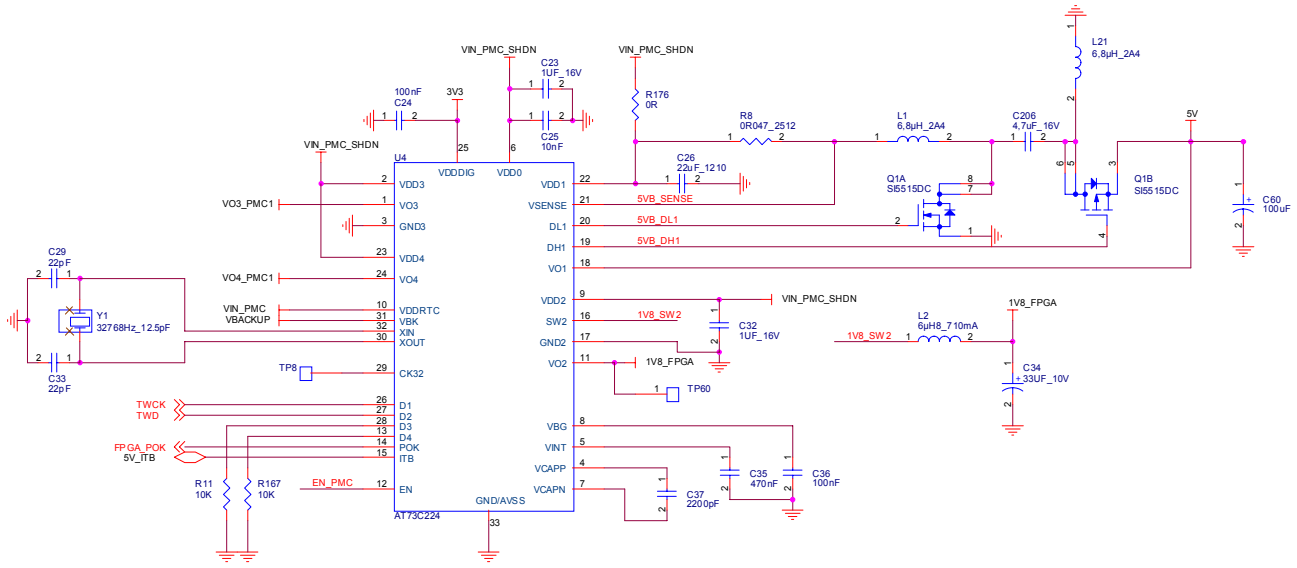
2.4.1.10.1 Power Supplies

Power supply of the board is assumed either by an external 5V/10W AC/DC sector adapter or Li-Ion external battery (VIN_PMC):

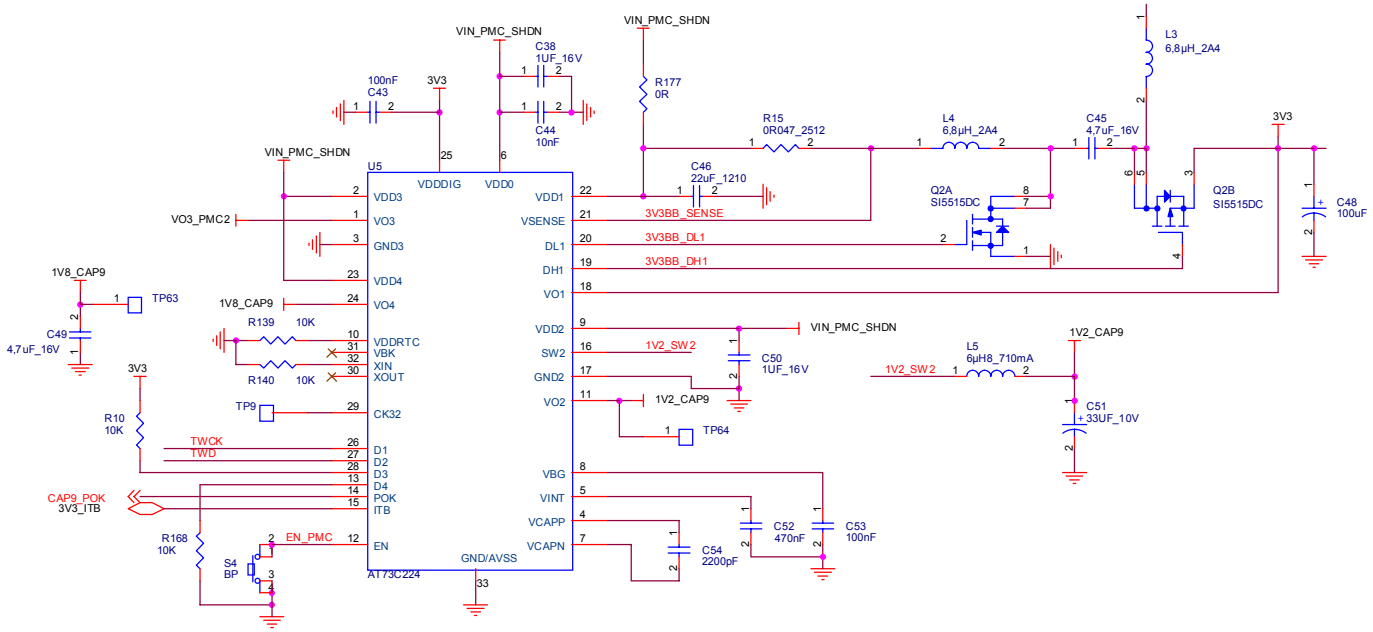


The different power supplies of the board are provided by two AT73C224 chips from the Atmel family of AT73 products (controlled by the AT91CAP9 TWI bus) and one LTC3412 as shown below:

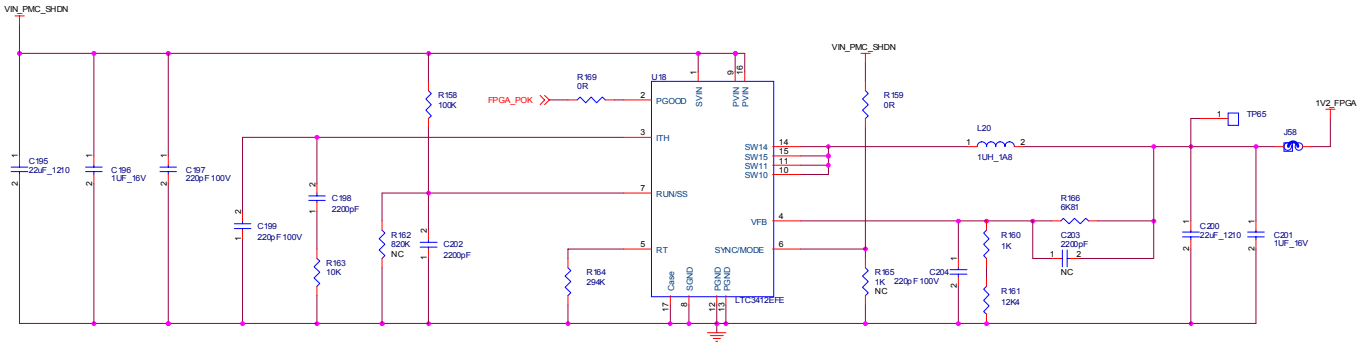
- First AT73C224
  - 5V/1A (SEPIC buck boost)
  - 1.8V_FPGA/500mA (boost)
  - 1.2V VBACKUP



- Second AT73C224
  - 3.3V/1AZ (SEPIC buck boost)
  - 1.2V_CAP9/500 mA (boost)
  - 1.8V_CAP9/200 mA (LDO)



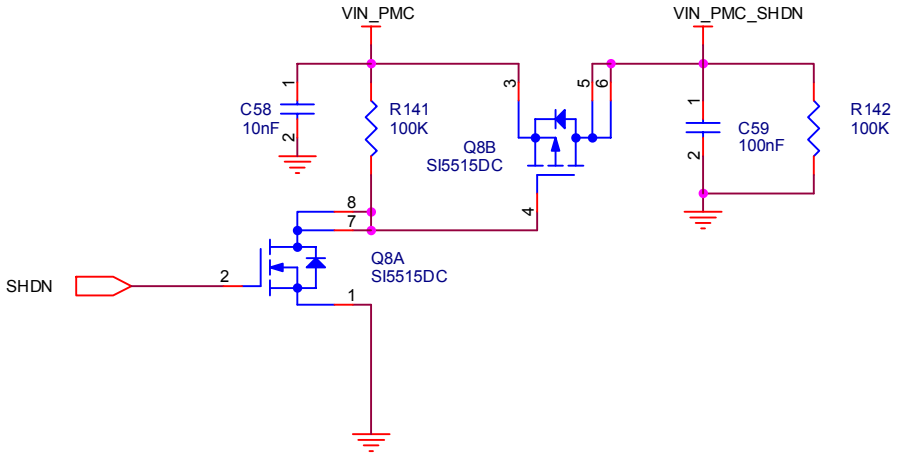
- LTC3412: 1.2V_FPGA/1A



2.4.1.10.2 Low-power Mode

The power supply of this 3 PMC (VIN_PMC_SHDN) is managed by the AT91CAP9 SHDN signal (power by VDDBU. (See “F12: RTC and Backup” on page 2-25.)

When AT91CAP9 commands low power mode, it drives it's SDHN pin low and so switches off the 3 PMC power supply. The implementation of the switch is shown below:



No external pull-up is required on the SHDN signal (even at start-up).

2.4.1.11 F11: Battery Charger

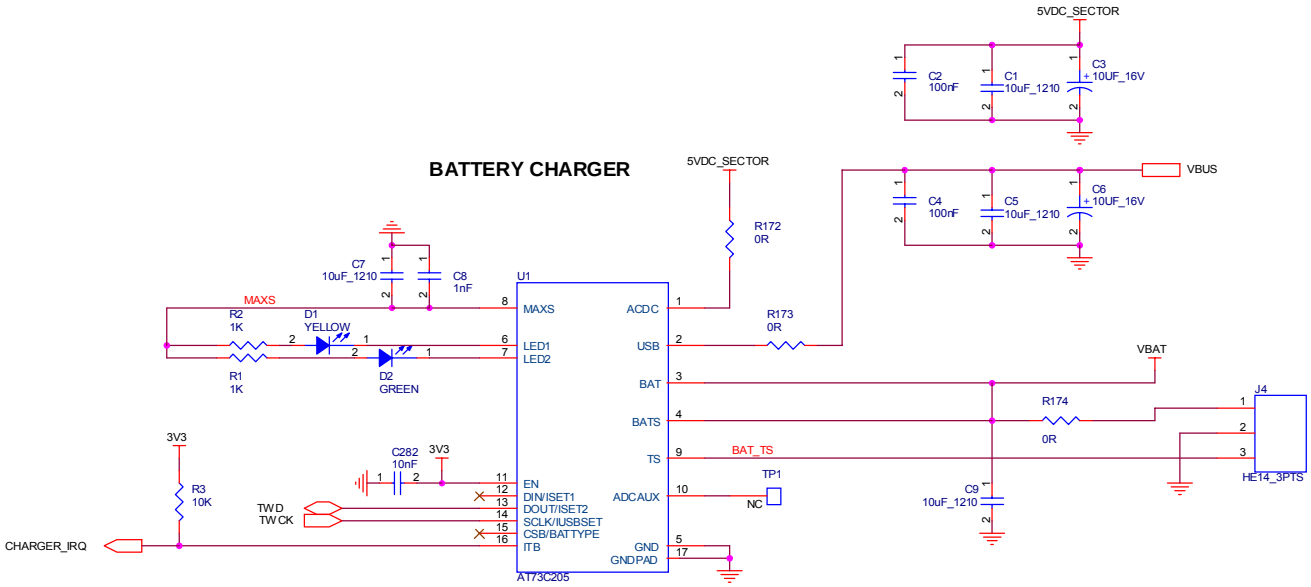
An Atmel AT73C205 stand alone battery charger is implemented on the board.

It manages the charge of an external Li-Ion battery plugs on the EI1 interface, from 5V AC/DC sector adapter or VBUS USB Device external power source.

The battery charger is controlled by the AT91CAP9 TWI bus.

Two LEDs (yellow and green) indicate the charge status.

The implementation of the AT73C205 battery charger is shown below.



2.4.1.12 F12: RTC and Backup

2.4.1.12.1 Backup

The first AT73C224 PMC provides a 3V VBACKUP power supply on its VBK power pin, from non-managed VIN_PMC supply on it's VDDRTC power in.

This VBACKUP power supply recharges a manganese-lithium rechargeable coin battery in the EI12 interface. It also supplies the AT73C239 chip on it's VBAT power pin, which generates (VO4 output) 1.2V_SAVE to supply the VDDBU AT91CAP9 power supply.

When no external power supplies are applied on the board, the AT73C239 is only supplied by the manganese-lithium rechargeable coin battery to maintain the VDDBU AT91CAP9 power supply

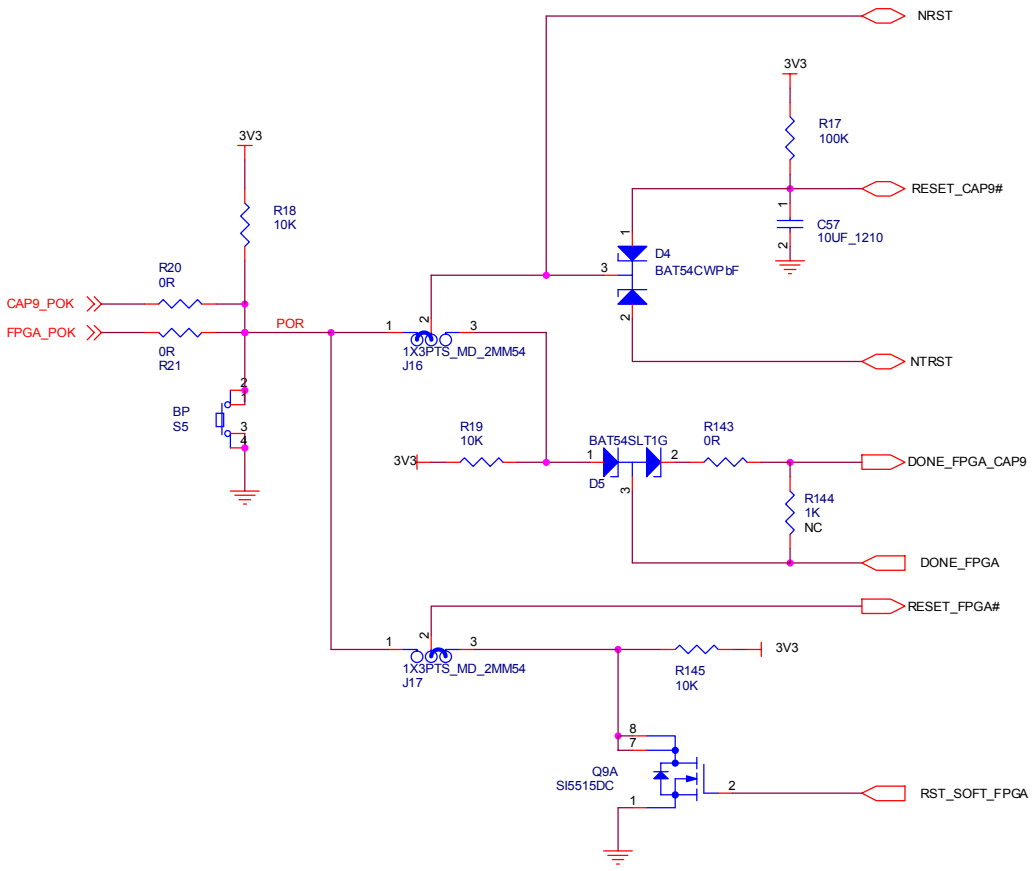
2.4.1.12.2 RTC

The first AT73C224 PMC described above integrates an RTC module with an external 32,768 kHz quartz connection. (See “First AT73C224” on page 2-23.)

The RTC module is powered by a non-managed VIN_PMC source on it's VDDRTC power pin. When no external power supplies are applied on the board, the RTC module is powered on it's VBK power pin by the manganese-lithium rechargeable coin battery, VBACKUP supply.

2.4.1.13 F13: Reset Configuration

Reset of the board is assumed by the reset circuit as shown below.



Each AT73C224 PMC provides an active low reset signal when an error occurs on one of it's power supply outputs. These open-drain output signals, CAP9_POK and FPGA_POK, with 10k to 3.3V pull-up, are connected to a push button for manual hardware reset and provide the POR signal.

Reset signals are:

- POR: Power On Reset signal, managed by CAP9_POK, FPGA_POK or manual hardware reset push button (active low)
- NRST: ICE probe AT91CAP9 microcontroller reset signal (active low)
- RESET_CAP9: AT91CAP9 microcontroller reset signal (active low)
- NTRST: test reset (active low)
- RESET_FPGA: FPGA reset signal, it drives the nCONFIG signal of the FPGA (active low)
- RST_SOFT_FPGA: FPGA reset from AT91CAP9 microcontroller (active high)

Two jumpers on the 3-pin connectors, J16 and J17 define reset configuration of the board and the way status reset signals are driven.

Status reset signals are:

- DONE_FPGA: the CONF_DONE FPGA configuration status signal
- DONE_FPGA_CAP9: indicates the FPGA configuration status to the AT91CAP9 microcontroller (PIO

Table 2-19. Reset Configuration

Reset Configuration	Reset Description	J16 Jumper Position	J17 Jumper Position
1	Uncontrolled reset-then-start CAP9 and FPGA order	1-2	1-2
2	Reset CAP9 resets FPGA, start CAP9 and then start FPGA	1-2	2-3
3	Reset FPGA resets CAP9, start FPGA and then start CAP9	2-3	1-2
4	Forbidden (no reset available)	2-3	2-3

2.4.1.14 F14: Programming and Configuration

2.4.1.14.1 JTAG Programming

Two different JTAG programming chains are implemented on the board:

- Stand-alone JTAG chains (default)

Each programmable device (microcontroller and FPGA) has it's own JTAG programming chain. (See "EI11: JTAG and Serial Configuration Interfaces" on page 2-7.)

  - ICE-JTAG chain for AT91CAP9 JTAG programming
  - USB-Blaster chain for FPGA JTAG programming

- ICE-only JTAG daisy chain

It's possible to use only the ICE-JTAG interface to program microcontroller and FPGA on a unique JTAG daisy chain. AT91CAP9 is the first device in the daisy chain, FPGA is the second one.

Configuration of the jumper positions must be as shown in the table that follows.

Table 2-20. Jumper Position Configuration

JTAG Programming Chain	J59 Jumper Position	J60 Jumper Position	J61 Jumper Position	J62 Jumper Position	J63 Jumper Position	J64 Jumper Position	Note
Stand-alone JTAG chains	1-2	2-3	2-3	2-3	2-3	2-3	Default chain
ICE-only JTAG daisy chain	2-3	1-2	1-2	1-2	1-2	1-2	-

2.4.1.14.2 Serial Device Configuration

Three ways can be used to program the FPGA EPCS16 serial device.

- Serial device configuration port

The FPGA EPCS16 serial device configuration can be programmed via the EI11 serial device configuration port with Altera USB Blaster probe.

- Altera SFL (Serial Flash Loader) function

In this case, the serial device is programmed via FPGA JTAG interface.

The **advantage** is that it makes it possible to configure the FPGA and program serial configuration devices using the same JTAG interface. The **disadvantage** is that programming is very slow because SFL needs to configure the FPGA before programming the serial configuration device.

- Microcontroller programs serial configuration device

In this case, the AT91CAP9 microcontroller drives the following signals via its PIO

Table 2-21. AT91CAP9 PIO Signal Control

Signal Name	Signal Description	AT91CAP9 I/O
nCE	Configuration Chip enable	PB6
nCSO	Configuration Chip select	PB3
DCLK	Configuration Clock pin	PB7
ASDO_FPGA	Configuration Read enable	PB8

To use this mode of programming, **R216 to R219 0Ω resistors must be mounted and reset configuration must be set to 2.** (See “F13: Reset Configuration” on page 2-26.)

Once the serial configuration device is programmed, FPGA configuration is initiated at start-up between FPGA and the serial configuration device via the DATA0, DCLK, nCSO and ASDO signals.

The FPGA AS mode configuration scheme is set by the MSEL[0..3] signals (default Fast AS).

Table 2-22. FPGA AS Mode Configuration

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0
Fast AS (40 MHz)	1	0	0	0
Remote system upgrade fast AS (40 MHz)	1	0	0	1
AS (20 MHz)	1	1	0	1
Remote system upgrade AS (20 MHz)	1	1	1	0

2.4.1.15 F15: Prototyping Area

Two prototyping areas are implemented on the board.

- The first one is a 20x18 points, 1.24 mm-pitch matrix, with two 1x8 points, 1.24 mm-pitch line, connected to 5V and 3.3V added on top of the matrix, and 1x20 points, 1.2 4 mm pitch line, connected to GND added on the bottom of the matrix.
- The second one is a 10x8 points, 2.54 mm-pitch matrix, with two 1x4points, 2.54 mm-pitch line, connected to 5V and 3.3V added on top of the matrix, and 1x8 points, 2.54 mm-pitch line, connected to GND added on the bottom of the matrix.

2.4.2 Physical Characteristics

2.4.2.1 Mechanical

The format of the CAP9-STK board is 185x120 mm.

2.4.2.1.1 LCD Panel Support

An LCD panel support is implemented on the board to receive the TX09D70VM1CCA Hitachi LCD.

2.4.2.1.2 BGA Socket

A 22.225x22.225 mm BGA socket can be implemented on the board to receive the AT91CAP9 400-ball LFBGA.

2.4.2.2 Electrical

The nominal consumption of the board is less than 10 W.

2.4.2.3 Environmental

No requirements are specified. However, the board is designed to run normally under 0°C to 55°C temperature.

All components mounted on the board are RoHS compliant.

2.4.2.4 Packaging

The CAP9-STK packaging includes the following items:

- The CAP9 Starter Kit Standalone Board wrapped in an ESD packaging.
- A CD of documentation and software, including software development tools and FPGA development tools
- The power supply of the board with adaptors for Europe, United Kingdom, China and United States
- A set of communication cables, including cables for USB, Ethernet and serial port.
- A manganese-lithium 3V rechargeable coin battery

Section 3

Board Strap and Switch Configuration

3.1 Connectors 1x2

Table 3-1. Connectors 1x2

Name	Position (default)	Descriptions		
		Closed		Open
J5	Not Connected	VIN_AT73C239 power supply is 5V if S1 in 1-3		VIN_AT73C239 power supply is VIN_SURV_AT73C239 if S1 is in 1-2 position.
J6[(1)]	Connector not Mounted	VIN_AT73C239 power supply is VIN_PMC if S1 is in 1-2 position and S2 is in 1-3 position.	VIN_SURV_AT73C239 power supply is 3V3 if S2 is in 1-2 position.	VIN_SURV_AT73C239 power supply is VIN_PMC if S2 is in 1-3 position.
J7	1-2	Reset out of AT73C239 (U3) if VIN_AT73C239 < 2.6V on FIQ# (Fast Interrupt) of CAP9		FIQ# = open (not used by CAP9)
J8	1-2	TP2 = VO1 of AT73C239 (U3)		Measure VO1 current of AT73C239 (U3) if a charge is connected between TP2 and TP.3
J9	1-2	TP4 = VO2 of AT73C239 (U3)		Measure VO2 current of AT73C239 (U3) if a charge is connected between TP4 and TP5.
J11	1-2	V_{BAT} of AT73C239 (U3) supply by VIN_AT73C239 if S9 is in 1-3 posotion.	V_{BAT} of AT73C239 (U3) is not connected.	V_{BAT} of AT73C239 (U3) supply by VBACKUP if S9 is in 1-2 postion.
J12	1-2	TP6 = VO3 of AT73C239 (U3)		Measure VO3 current of AT73C239 (U3) if a charge is connected between TP6 and TP7.
J20	1-2	V_{DDCORE} supply by 1V2		V_{DDCORE} is off.
J21	1-2	V_{DDIOM} supply by 1V8		V_{DDIOM} is off.
J22	1-2	V_{DDPLL} supply by 3V3		VDDPLL is off.
J23	1-2	V_{DDIOP0} supply by 3V3		V_{DDPLL} is off.
J24	1-2	V_{DDIOP1} supply by 3V3 if R26 is connected but R27 is not connected. V_{DDIOP1} supply by 1V8 if R27 is connected but R26 is not connected.		V_{DDIOP1} is off.
J25	1-2	V_{DDUPLL} supply by 1V2		V_{DDUPLL} is off.
J26	1-2	$V_{DDUTMIC}$ supply by 1V2		$V_{DDUTMIC}$ is off.
J27	1-2	$V_{DDUTMII}$ supply by 3V3		$V_{DDUTMII}$ is off.
J29	1-2	V_{DDANA} supply by 3V3 filtered		V_{DDANA} is off.
J39	1-2	Chip select audio DAC (U12) by CAP9		The audio DAC (U12) not selected.

Table 3-1. Connectors 1x2 (Continued)

Name	Position (default)	Descriptions	
		Closed	Open
J44	1-2	Chip select SPI DATA FLASH (U17) by CAP9	The SPI DATA FLASH (U17) not selected
J48	1-2	TP24 = VO3_PMC1 of AT73C224 (U4)	Measure VO3_PMC1 current of AT73C224 (U4) if a charge is connected between TP24 and TP25
J49	1-2	TP26 = VO4_PMC1 of AT73C224 (U4)	Measure VO4_PMC1 current of AT73C224 (U4) if a charge is connected between TP26 and TP27
J50	1-2	TP28 = VO3_PMC2 of AT73C224 (U5)	Measure VO3_PMC2 current of AT73C224 (U5) if a charge is connected between TP28 and TP29
J58	1-2	1V2_FPGA is connected	1V2_FPGA is off
J66	1-2	Flash NAND CE# signal is driven by FN_CE# CAP9 signal	Flash NAND CE# signal is pull-up to 1V8
J67	1-2	1V2_FPGA is connected	1V8_FPGA is off

Note: 1. J6 connector is not mounted on the prototype.

3.2 Connectors 1x3

Table 3-2. Connectors 1x3

Name	Position (default)	Descriptions	
		1-2	2-3
J16	1-2	POR (manually or AT73C224) resets the CAP9	Reset sthe CAP9 during the programming of FPGA
J17	2-3	POR (manually or AT73C224) resets the FPGA	Resest the FPGA by CAP9 software
J28	1-2	VDDBU supply by 1V2_SAVE	VDDBU supply by 1V2
J31	1-2	BMS pull-up to 3V3	BMS tied to GND
J52	1-2	Analog input 1 on CAP9 ADC channel 4	Analog input 1 on CAP9 ADC channel 0
J53	1-2	Analog input 2 on CAP9 ADC channel 5	Analog input 2 on CAP9 ADC channel 1
J54	1-2	Analog input 3 on CAP9 ADC channel 6	Analog input 3 on CAP9 ADC channel 2
J55	1-2	Analog input 4 on CAP9 ADC channel 7	Analog input 4 on CAP9 ADC channel 3
J59	1-2	TDO ICE port signal is CAP9 TDO signal (with J60 on 2-3).	FPGA TDI signal is CAP9 TDO signal (with J64 on 1-2).
J60	2-3	TDO ICE port signal is FPGA TDO signal (with J63 on 1-2).	TDO ICE port signal is CAP9 TDO signal (with J59 on 1-2).
J61	2-3	FPGA TMS JTAG signal is ICE port TMS signal.	FPGA TMS JTAG signal is FPGA JTAG port TMS signal.
J62	2-3	FPGA TCK JTAG signal is ICE port TCK signal.	FPGA TCK JTAG signal is FPGA JTAG port TCK signal.
J63	2-3	TDO ICE port signal is FPGA TDO signal (with J60 on 1-2).	FPGA JTAG port TDO signal is FPGA JTAG TDO signal.
J64	2-3	FPGA TDI JTAG signal is CAP9 TDO signal (with J59 on 2-3).	FPGA JTAG TDI signal is FPGA JTAG port TDI signal.

3.3 Switches

Table 3-3. Switches

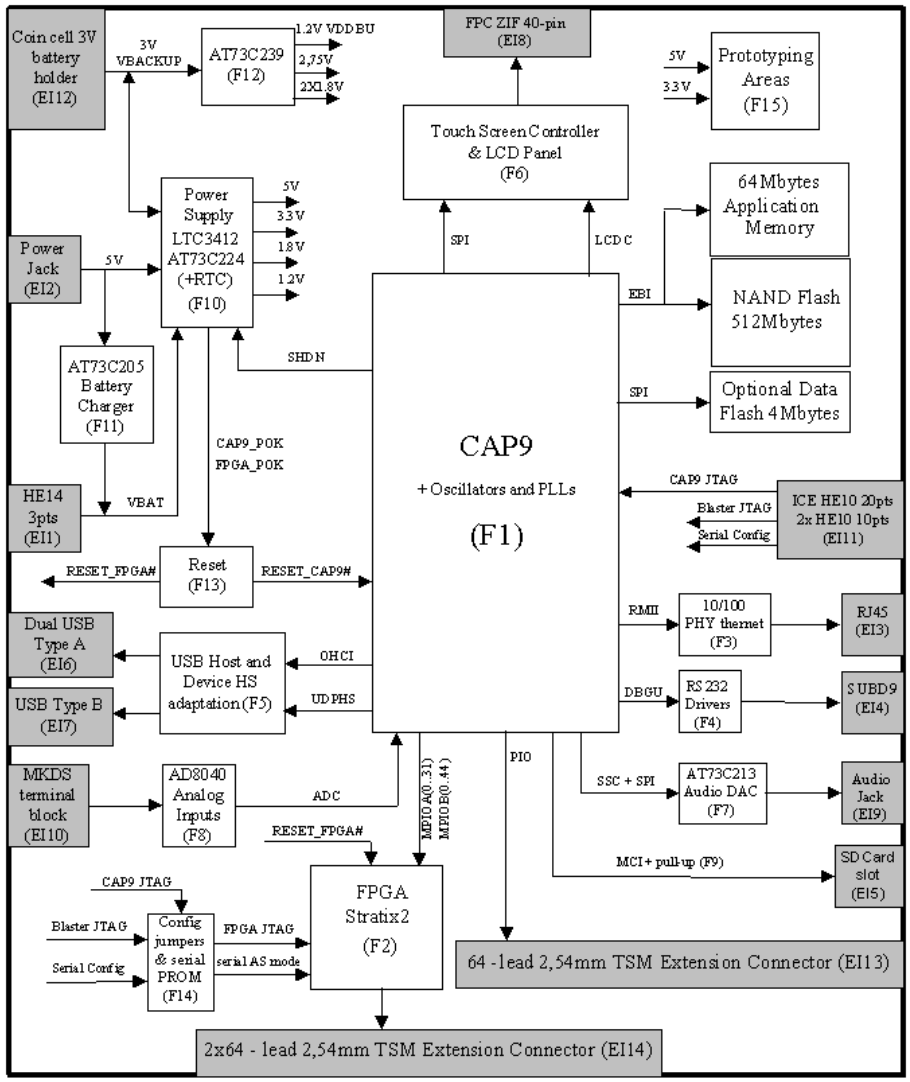
Name	Position (default)	Descriptions	
		1-2	1-3
S1	1-3	VIN_AT73C239 power supply is VIN_SURV_AT73C239 power supply.	VIN_AT73C239 power supply is 5V if J5 is connected. Not connected by default for AT73C239 (connected for AT73C237 mounting).
S2	1-3	VIN_SURV_AT73C239 power supply is 3V3 power supply.	VIN_SURV_AT73C239 power supply is VBACKUP (J6 connector not mounted, VBACKUP strap on S2 pin 3).
S7	1-2	AT73C239 TWCK signal is pull -up to VIN_SURV_AT73C239 and controlled by CAP9 PA7 PIO (allows hibernate mode).	AT73C239 TWCK signal is CAP9 I2C bus TWCK signal.
S8	1-2	AT73C239 TWCK signal is VIN_SURV_AT73C239 power supply.	AT73C239 TWD signal is CAP9 I2C bus TWD signal.
S9	1-2	AT73C239 V_{BAT} power supply is V_{BACKUP}	AT73C239 V_{BAT} power supply is VIN_AT73C239 power supply.

Section 4

AT91CAP9-STK Schematics

4.1 This section contains the following appended schematics

- Top View
- Battery Charger and Backup
- PMC AT73C224
- Power Switch and Reset
- FPGA Core Supply
- IO Connectors and Proto Area
- CAP9 Power
- EBI and PIO
- System USB Clock
- FPGA Power
- FPGA IO Bank
- FPGA IO Bank
- FPGA Clock and Configuration
- Debug
- Ethernet SMSC
- USB Host and Device
- Audio
- Analog
- LCD and TSC
- SDCARD
- SDRAM, NAND and DataFlash



PAGE 01 : TITLE
PAGE 02 : TOP VIEW
PAGE 03 : BATTERY CHARGER & BACKUP
PAGE 04 : PMC AT73C224
PAGE 05 : POWER SWITCH & RESET
PAGE 06 : FPGA CORE SUPPLY
PAGE 07 : IO CONNECTORS & PROTO AREA
PAGE 08 : CAP9 POWER
PAGE 09 : EBI & PIO
PAGE 10 : SYSTEM USB CLOCK
PAGE 11 : FPGA POWER
PAGE 12 : FPGA IO BANK
PAGE 13 : FPGA CLOCK & CONFIG
PAGE 14 : DEBUG
PAGE 15 : ETHERNET SMSC
PAGE 16 : USB HOST & DEVICE
PAGE 17 : AUDIO
PAGE 18 : ANALOG
PAGE 19 : LCD & TSC
PAGE 20 : SDCARD
PAGE 21 : SDRAM, NAND & DATAFLASH

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C02	21/05/08	OBO	Création

Projet / Project: CAP9-STK

Schéma électronique / Schematic: TITLE

Format: A3 | Dessinateur / Drawer: O. Boitet | Référence / Reference: ADEC101389001 | Rév.: C02

Date: Tuesday, May 20, 2008 | Page 1 de / of 21

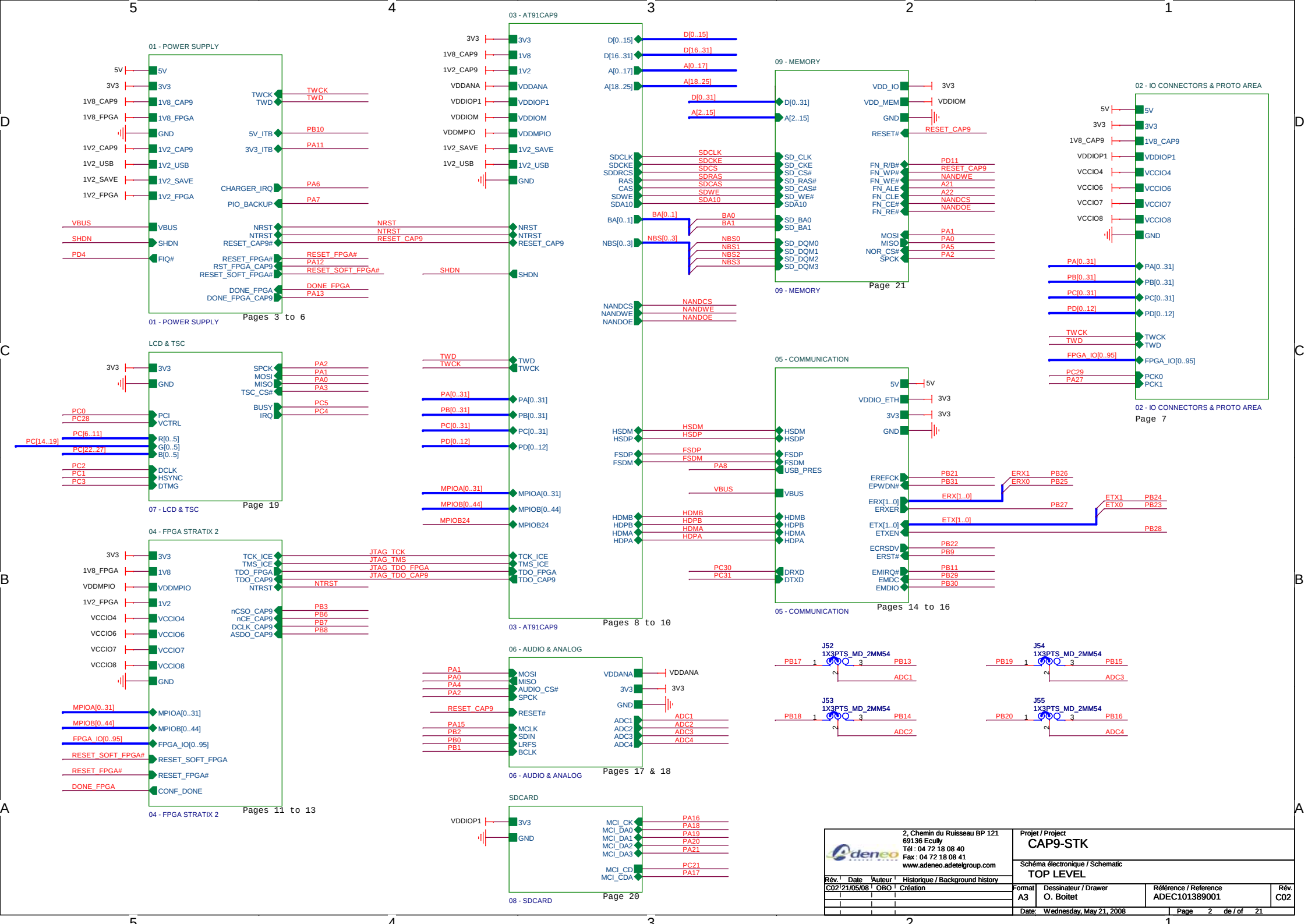

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Schéma électronique / Schematic: TOP LEVEL

Format	Dessinateur / Drawer	Référence / Reference	Rév.
A3	O. Boitet	ADEC101389001	C02

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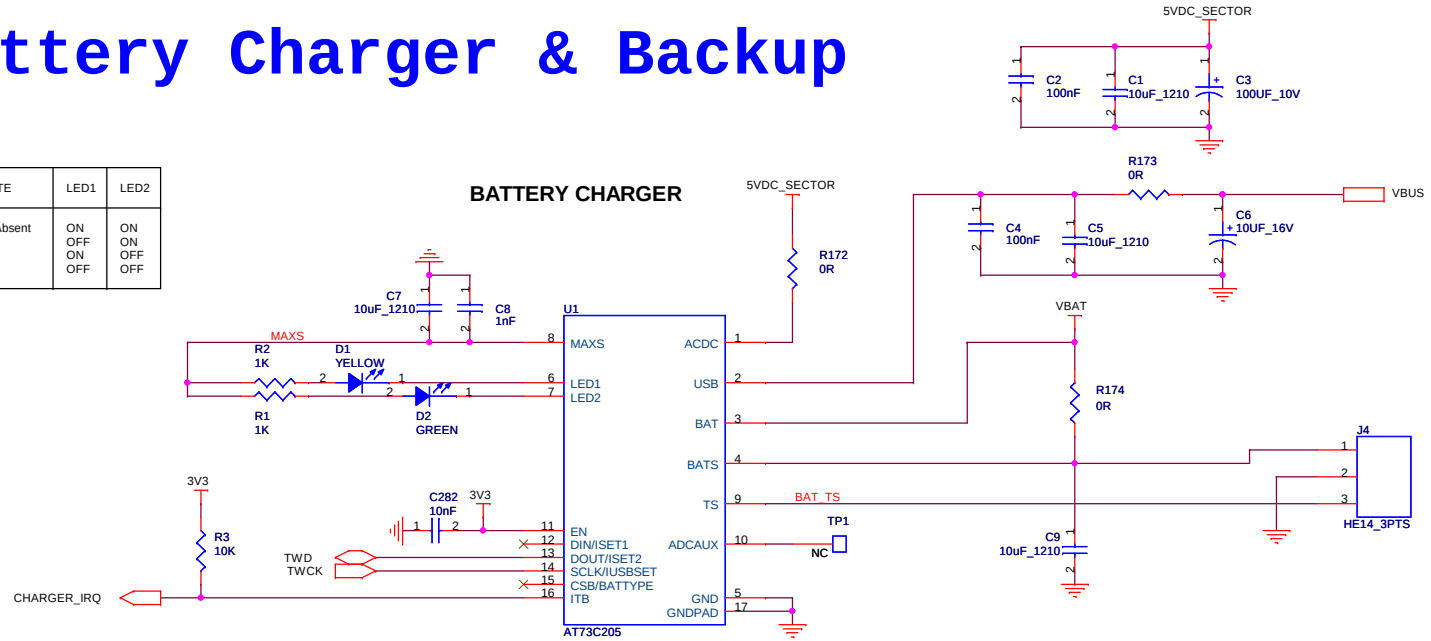
Battery Charger & Backup

1V2_SAVE ——— 1V2_SAVE

CHARGE STATE	LED1	LED2
Time out or Battery Absent	ON	ON
Charge complete	OFF	ON
Charge progressing	ON	OFF
Low Power Supply	OFF	OFF

BATTERY CHARGER



BACKUP

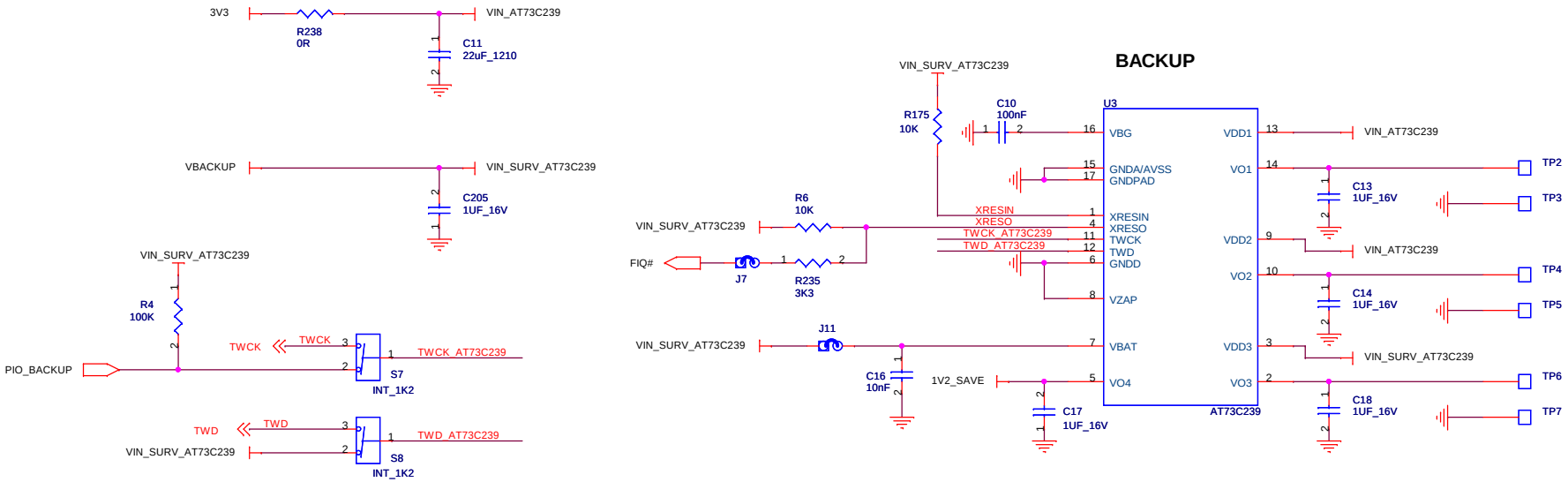


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Schéma électronique / Schematic: BATTERY CHARGER & BACKUP

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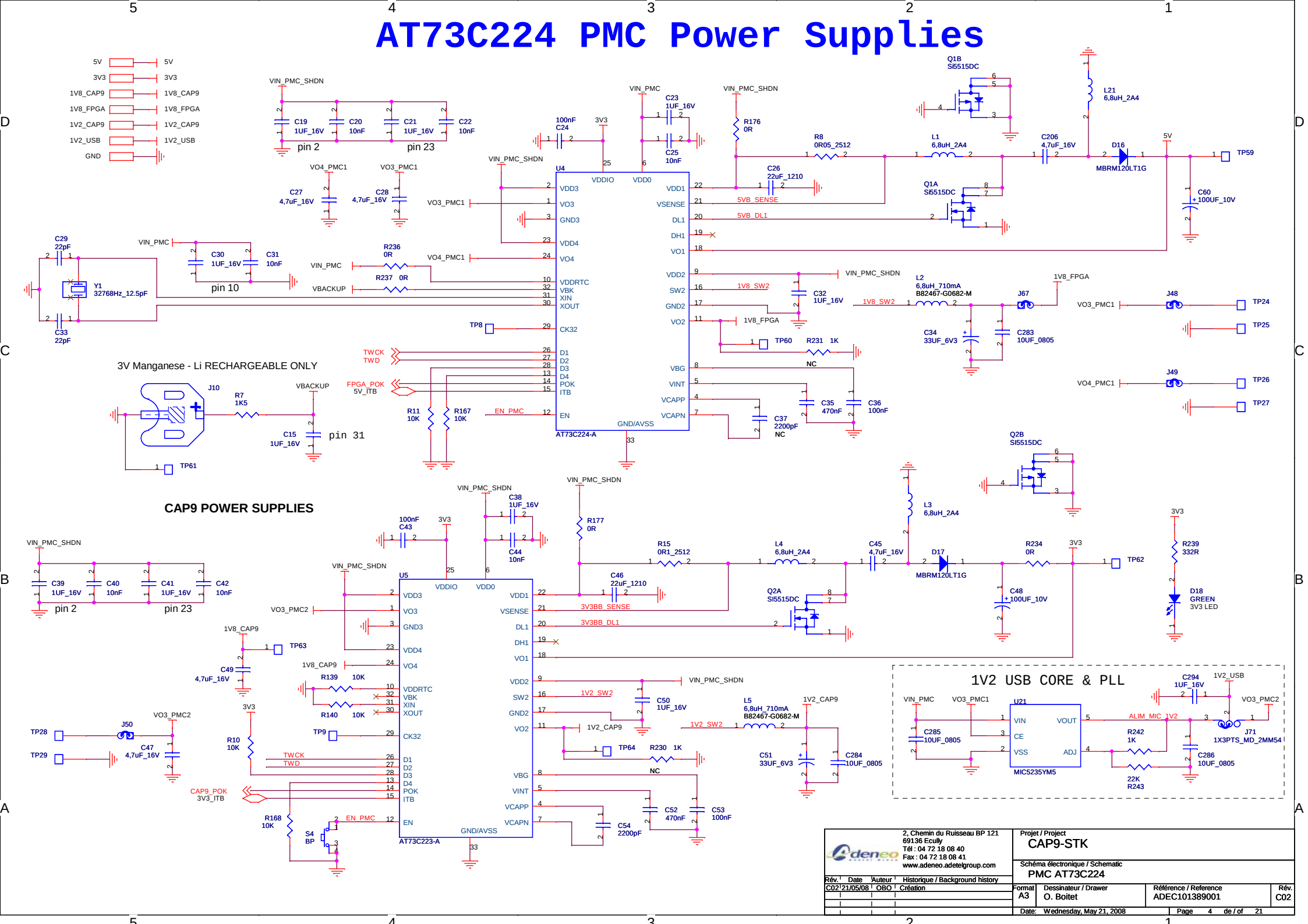
AT73C224 PMC Power Supplies



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Projet / Project: CAP9-STK

Schéma électronique / Schematic: PMC AT73C224

Format: A3

Dessinateur / Drawer: O. Boitet

Référence / Reference: ADEC101389001

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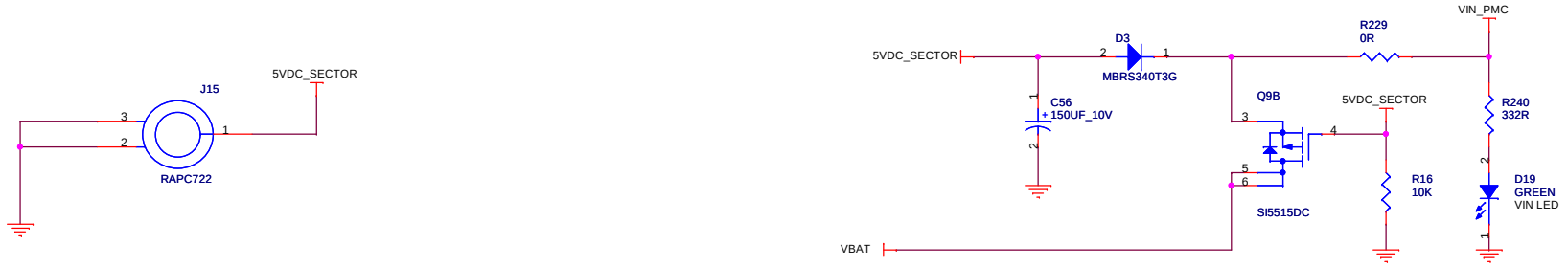
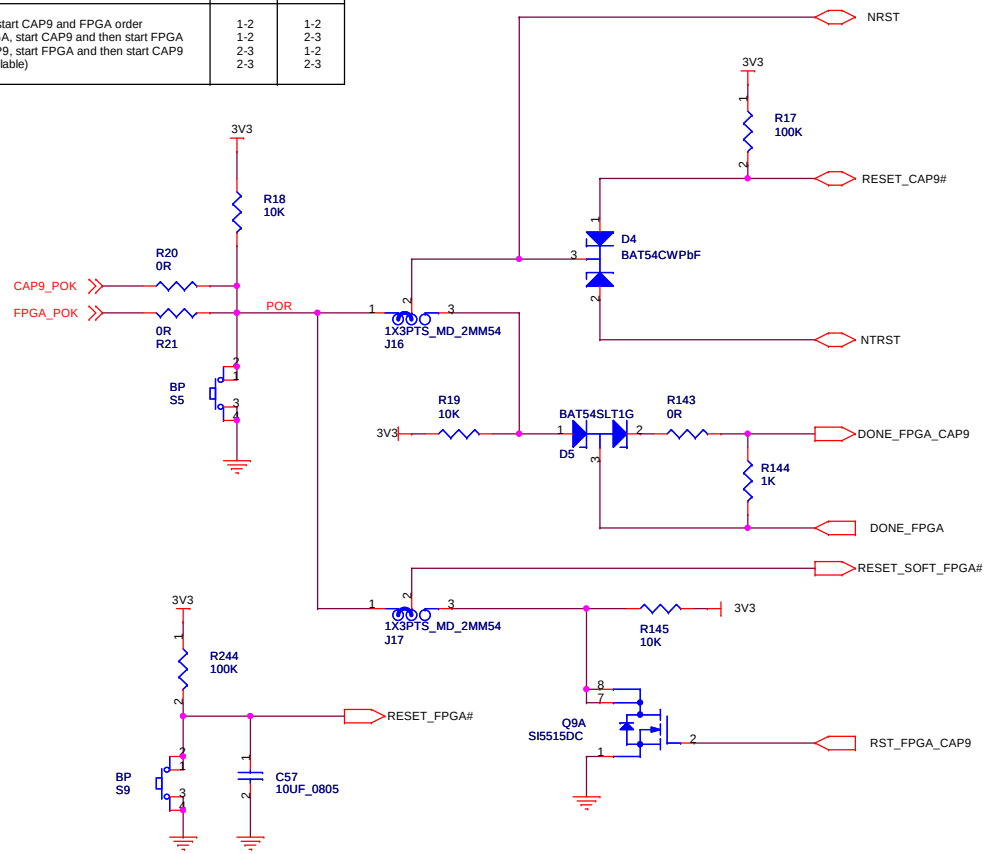
Power Switch & Reset

SWITCH 5VDC_SECTOR - VBAT

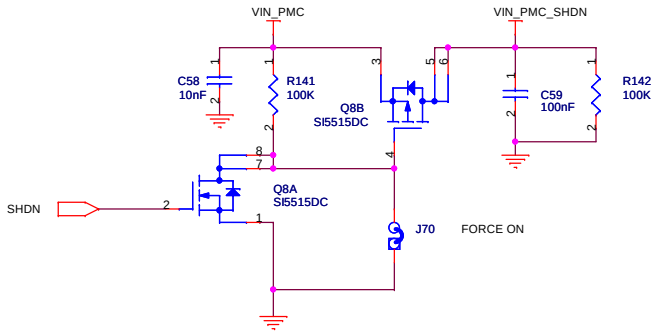


RESET CONFIG	J16 jumper	J17 jumper
Uncontroled reset then start CAP9 and FPGA order	1-2	1-2
Reset CAP9 resets FPGA, start CAP9 and then start FPGA	1-2	2-3
Reset FPGA resets CAP9, start FPGA and then start CAP9	2-3	1-2
Forbidden (no reset available)	2-3	2-3

RESET CONTROL



SHUTDOWN VIN_PMC



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Projet / Project: CAP9-STK

Schéma électronique / Schematic: POWER SWITCH & RESET

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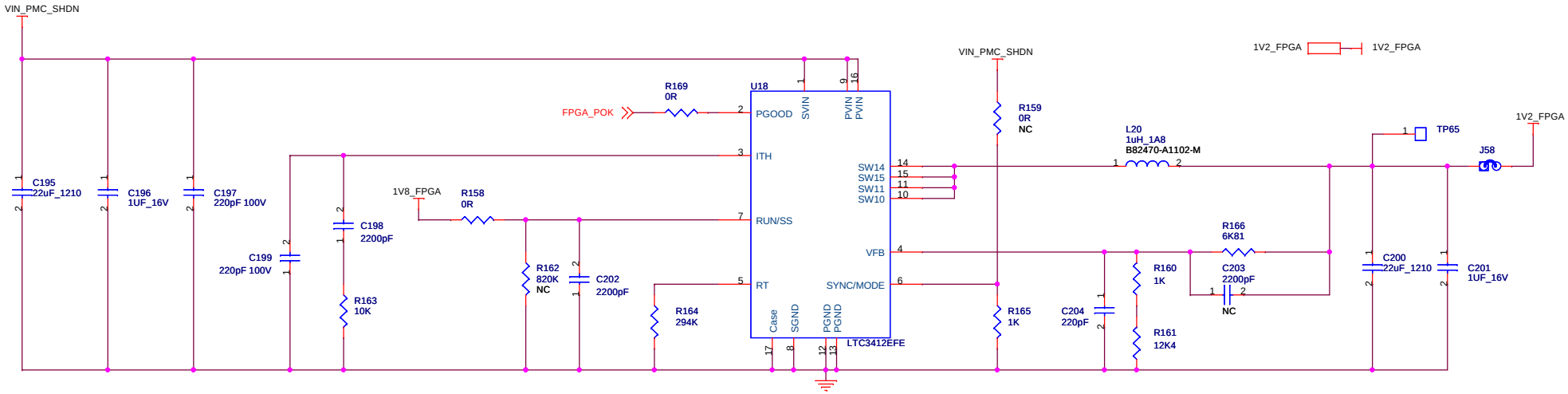
A3	O. Boitet	ADEC101389001	C02

Date: Wednesday, May 21, 2008

FPGA Core Supply



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	Date: Tuesday, May 20, 2008		Page 6 de / of 21

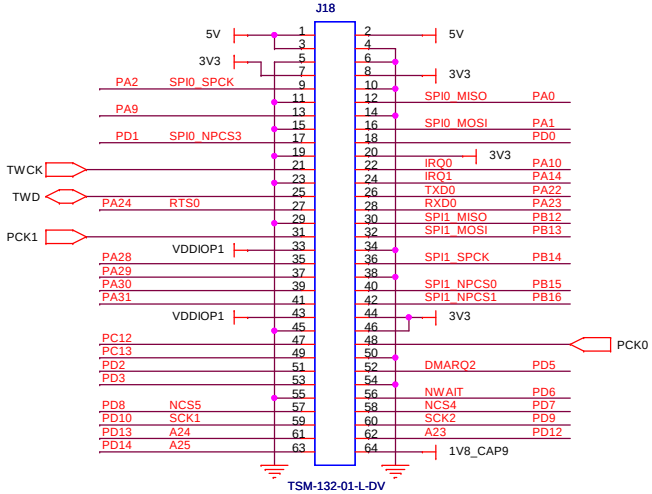
CAP9 & FPGA PIO Connectors

1V8_CAP9 — 1V8_CAP9
3V3 — 3V3
VDDIOP1 — VDDIOP1
5V — 5V
GND
TP66

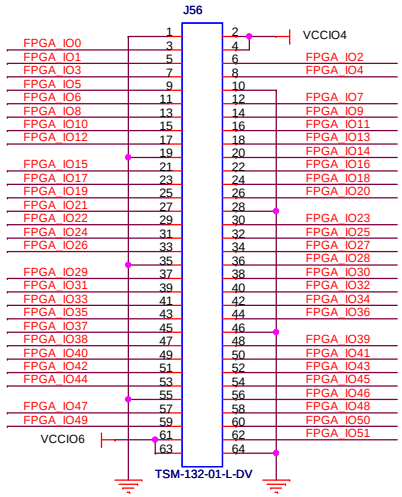
FPGA_IO[0..95] — FPGA_IO[0..95]
PA[0..31] — PA[0..31]
PB[0..31] — PB[0..31]
PC[0..31] — PC[0..31]
PD[0..12] — PD[0..12]

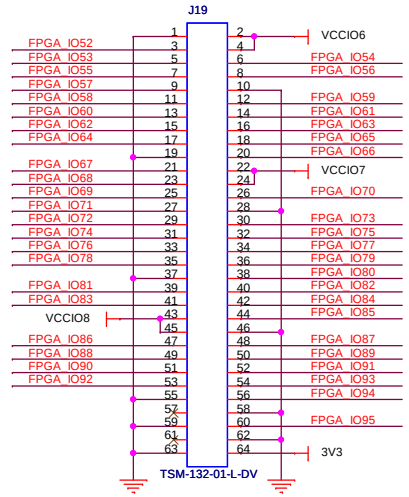
VCCIO4 — VCCIO4
VCCIO6 — VCCIO6
VCCIO7 — VCCIO7
VCCIO8 — VCCIO8

CAP9 PIO CONNECTOR

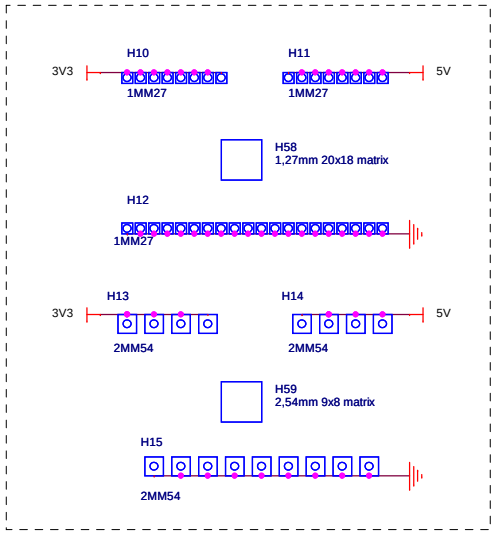


FPGA PIO CONNECTORS





USER'S GRID AREA



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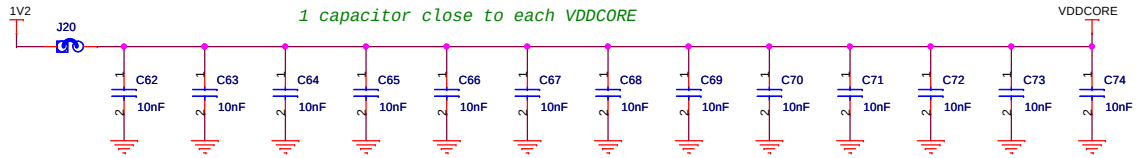
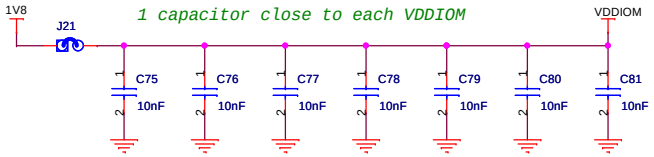
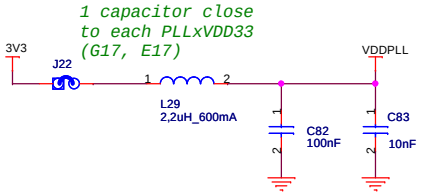
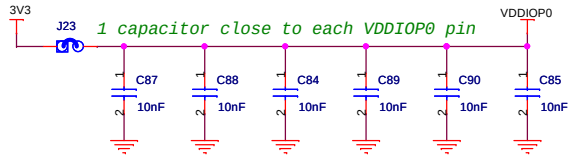
Projet / Project: CAP9-STK
Schéma électronique / Schematic: IO CONNECTORS & PROTO AREA
Format: A3
Dessinateur / Drawer: O. Boitet
Référence / Reference: ADEC101389001
Rév.: C02
Date: Wednesday, May 21, 2008

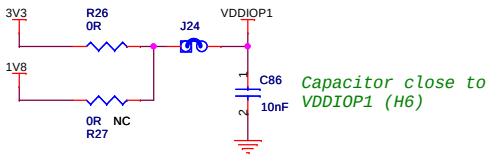
CAP9 - Power supply

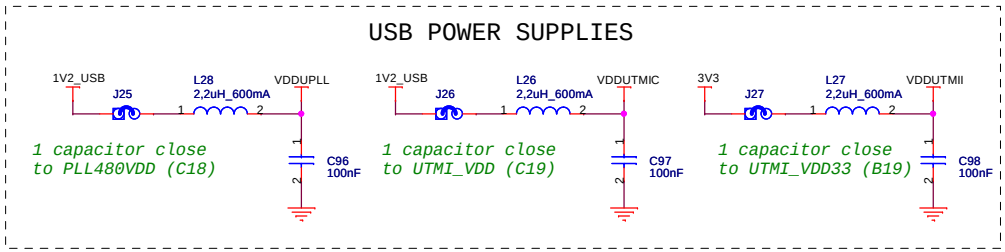


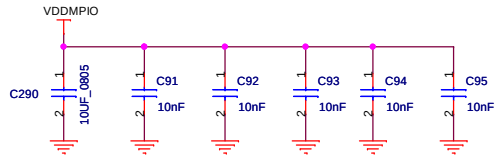


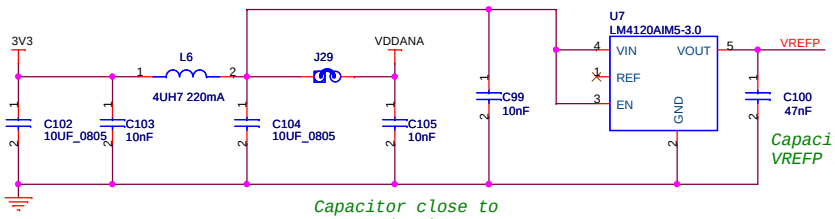


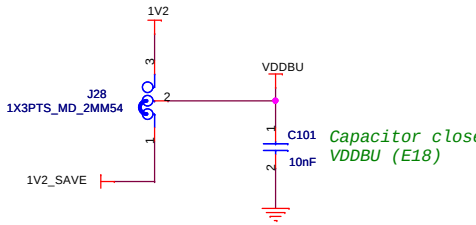


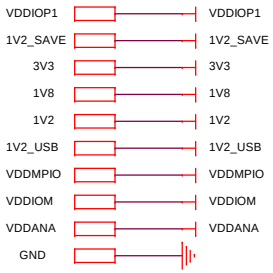


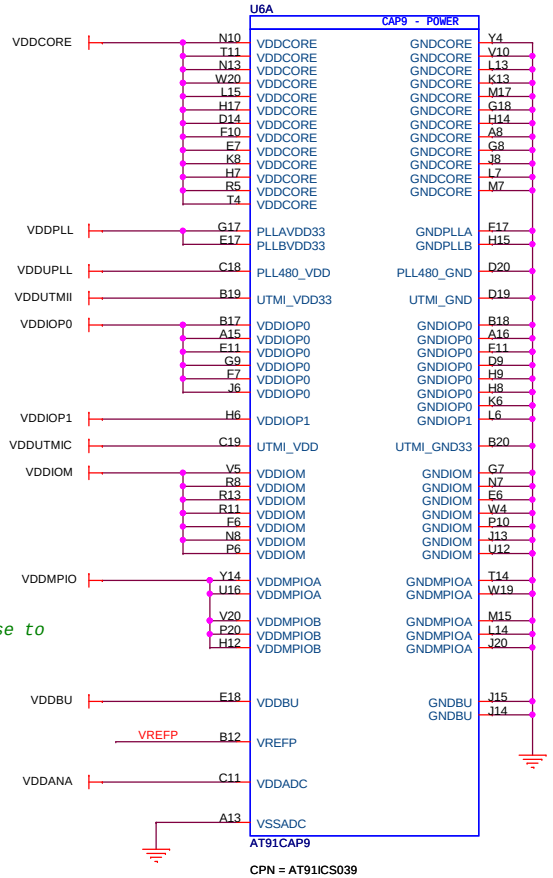












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Projet / Project: CAP9-STK

Schéma électronique / Schematic: CAP9 POWER

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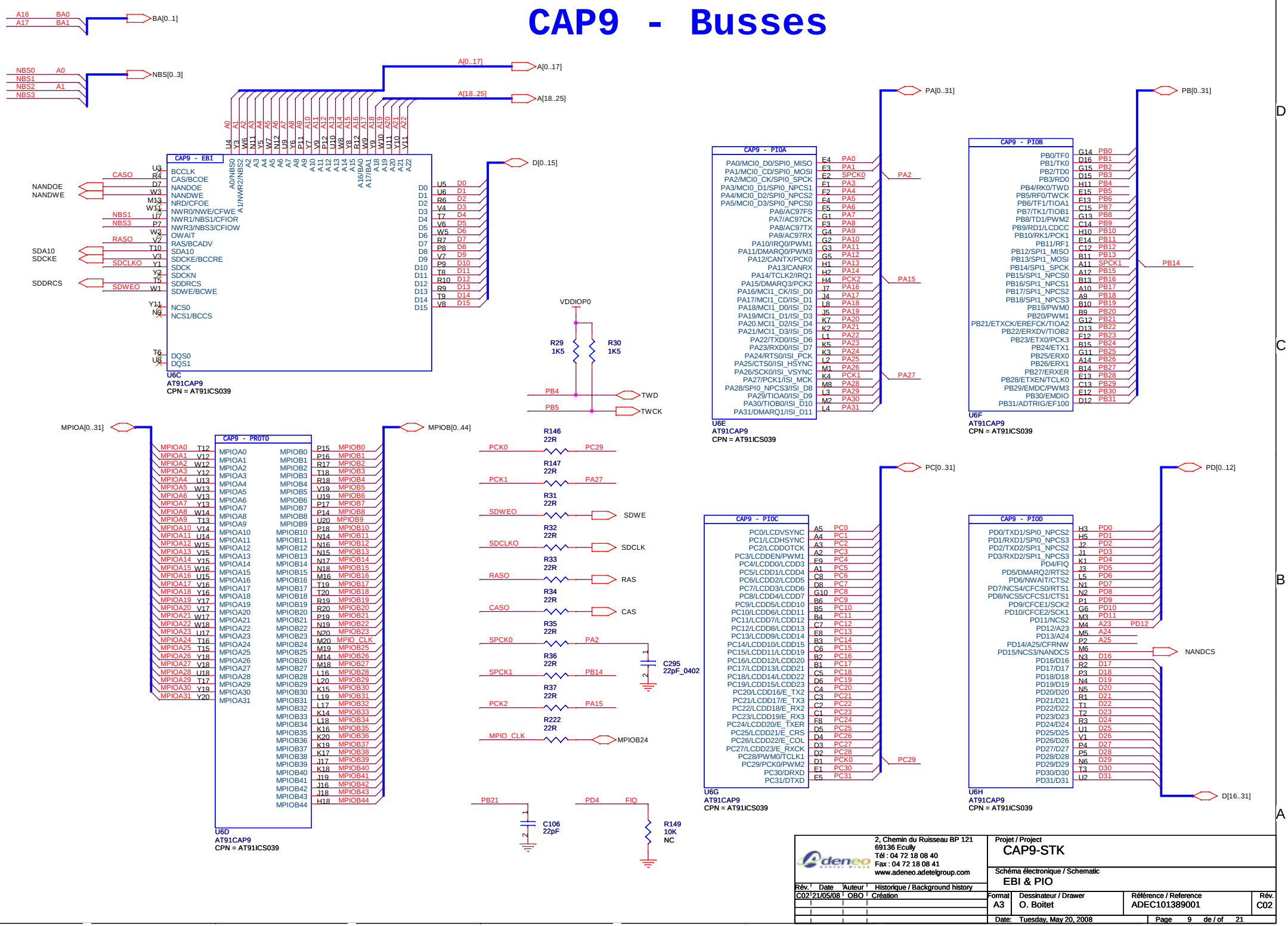
Date: Tuesday, May 20, 2008

CAP9 - Busses



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Projet / Project: CAP9-STK

Schéma électronique / Schematic: EBI & PIO

Format	Dessinateur / Drawer	Référence / Reference	Rév.
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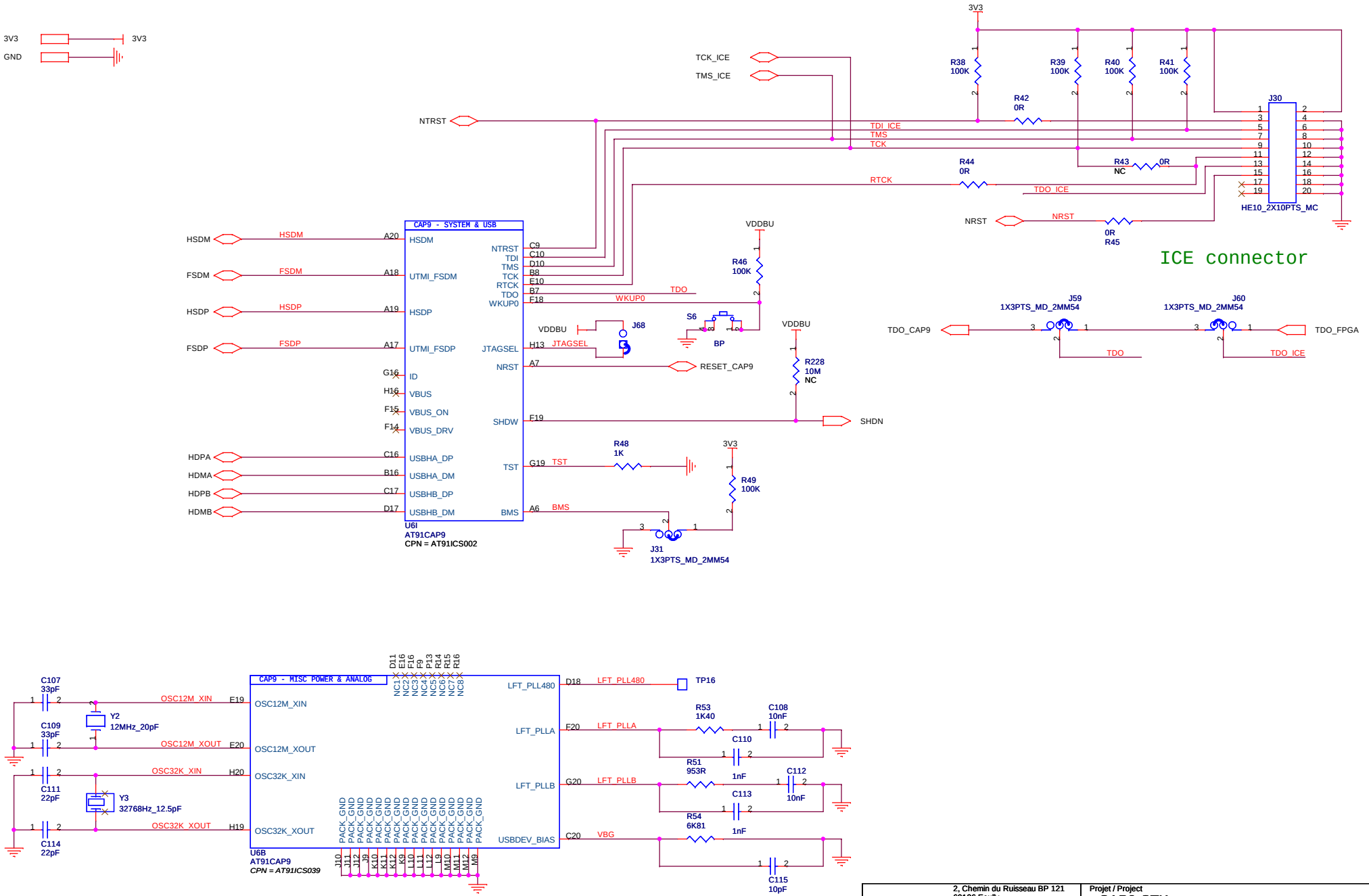
CAP9 - USB, PLL, ICE



Adeneo Embedded	2, Chemin du Ruisseau BP 121 69136 Ecully Tél : 04 72 18 08 40 Fax : 04 72 18 08 41 www.adeneo.adetelgroup.com	Projet / Project	CAP9-STK
		Schéma électronique / Schematic	SYSTEM USB CLOCK

Rév.	Date	Auteur	Historique / Background history
C02	21/05/08	OBO	Création

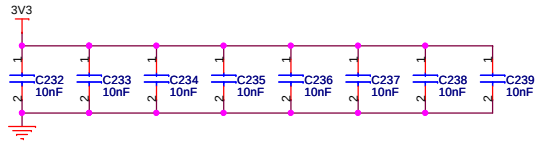
Format	Dessinateur / Drawer	Référence / Reference	Rév.
A3	O. Boitet	ADEC101389001	C02

Date: Tuesday, May 20, 2008 — Page 10 de / of 21

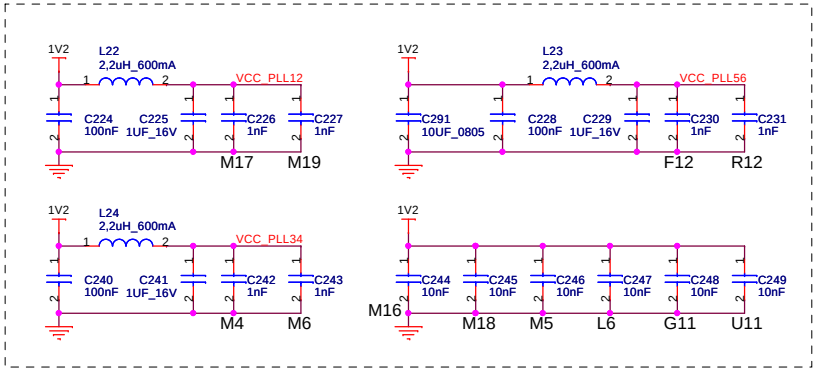
FPGA Power

3V3 3V3
1V8 1V8
1V2 1V2
VDDMPIO VDDMPIO
VCCIO4 VCCIO4
VCCIO6 VCCIO6
VCCIO7 VCCIO7
VCCIO8 VCCIO8
GND

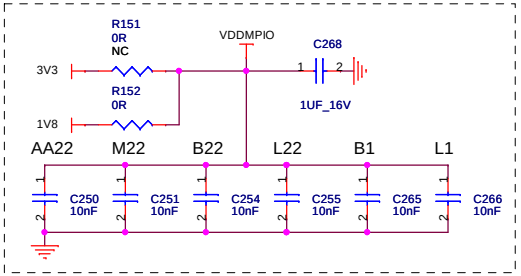
JTAG POWER SUPPLY



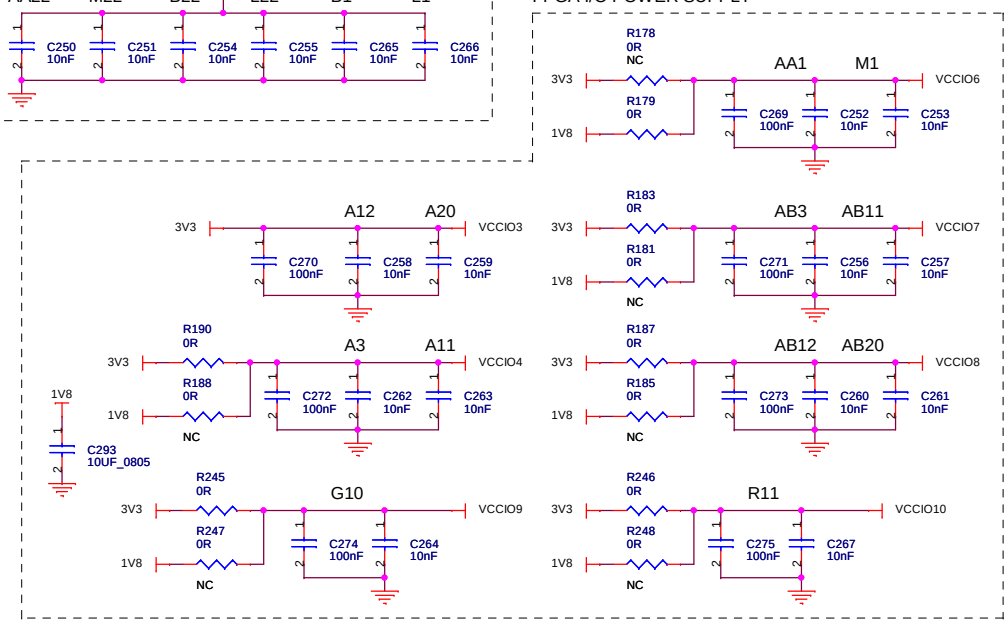
PLL POWER SUPPLY

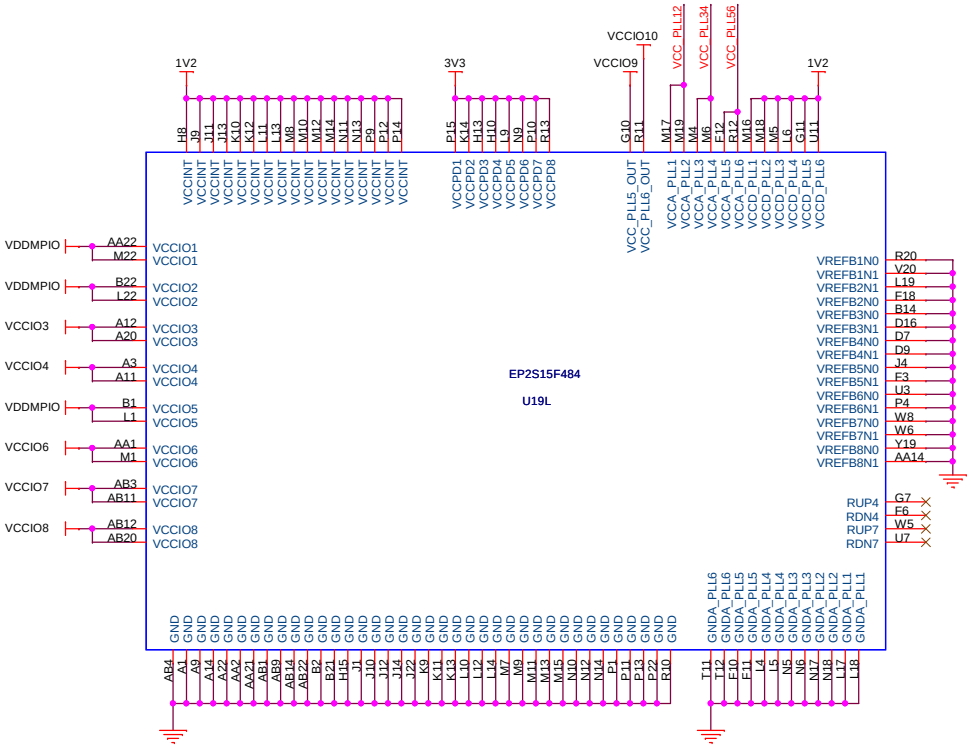


MPIO POWER SUPPLY

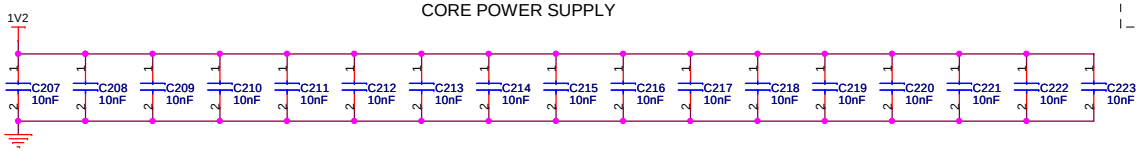


FPGA I/O POWER SUPPLY





CORE POWER SUPPLY



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Rév.	Date	Auteur	Historique / Background history
C02	21/05/08	OBO	Création

Projet / Project: CAP9-STK
Schéma électronique / Schematic: FPGA POWER
Format: A3
Dessinateur / Drawer: O. Boitet
Référence / Reference: ADEC101389001
Rév.: C02
Date: Wednesday, May 21, 2008

FPGA IO Bank

MPIOA[0..31] MPIOA[0..31]
MPIOB[0..44] MPIOB[0..44]
FPGA_IO[0..95] FPGA_IO[0..95]

MPIOB24 MPIOB24

MPIO BUS

U19A BANK1
EP2S15F484

		IO_VREFB1N0_R19	R19	MPIOA0	
		IO_VREFB1N0_R22	R22	MPIOA1	
P21	IO_VREFB1N0_P21	IO_VREFB1N0_T22	T22	MPIOA2	
P20	IO_VREFB1N0_P20	IO_VREFB1N0_U22	U22	MPIOA3	
N16	IO_VREFB1N0_N16	IO_VREFB1N1_T19	T19	MPIOA4	
N15	IO_VREFB1N0_N15	IO_VREFB1N0_T21	T21	MPIOA5	
MPIOA31 U17	IO_VREFB1N1_U17	IO_VREFB1N0_R21	R21	MPIOA6	
MPIOA30 W20	IO_VREFB1N1_W20	IO_VREFB1N0_U21	U21	MPIOA7	
MPIOA29 P17	IO_VREFB1N0_P17	IO_VREFB1N1_T20	T20	MPIOA8	
MPIOA28 U18	IO_VREFB1N1_U18	IO_VREFB1N0_P19	P19	MPIOA9	
MPIOA27 T17	IO_VREFB1N1_T17	IO_VREFB1N1_T18	T18	MPIOA10	
MPIOA26 U20	IO_VREFB1N1_U20	IO_VREFB1N1_R17	R17	MPIOA11	
MPIOA25 R16	IO_VREFB1N1_R16	IO_VREFB1N1_V22	V22	MPIOA12	
MPIOA24 P16	IO_VREFB1N0_P16	IO_VREFB1N1_U19	U19	MPIOA13	
MPIOA23 V18	IO_VREFB1N1_V18	IO_VREFB1N1_V21	V21	MPIOA14	
MPIOA22 Y22	IO_VREFB1N1_Y22	IO_VREFB1N1_W22	W22	MPIOA15	
MPIOA21 W19	IO_VREFB1N1_W19	IO_VREFB1N0_P18	P18	MPIOA16	
MPIOA20 V19	IO_VREFB1N1_V19	IO_VREFB1N0_R18	R18	MPIOA17	
		IO_VREFB1N1_W21	W21	MPIOA18	
		IO_VREFB1N1_Y21	Y21	MPIOA19	

U19B BANK2
EP2S15F484

MPIOB0 C22	IO_VREFB2N0_C22	IO_VREFB2N0_D21	D21	MPIOB25	
MPIOB18 F19	IO_VREFB2N1_F19	IO_VREFB2N1_K18	K18	MPIOB26	
MPIOB2 E20	IO_VREFB2N0_C20	IO_VREFB2N0_H19	H19	MPIOB27	
MPIOB4 G20	IO_VREFB2N0_G20	IO_VREFB2N1_J19	J19	MPIOB28	
MPIOB7 F20	IO_VREFB2N0_F20	IO_VREFB2N0_E21	E21	MPIOB29	
MPIOB8 K15	IO_VREFB2N1_K15	IO_VREFB2N0_H20	H20	MPIOB30	
MPIOB9 G17	IO_VREFB2N0_G17	IO_VREFB2N1_J18	J18	MPIOB31	
MPIOB10 H17	IO_VREFB2N0_H17	IO_VREFB2N1_K19	K19	MPIOB32	
MPIOB11 L15	IO_VREFB2N1_L15	IO_VREFB2N1_J20	J20	MPIOB33	
MPIOB12 D22	IO_VREFB2N0_D22	IO_VREFB2N1_K17	K17	MPIOB34	
MPIOB13 L16	IO_VREFB2N1_L16	IO_VREFB2N1_K21	K21	MPIOB35	
MPIOB14 K16	IO_VREFB2N1_K16	IO_VREFB2N1_G21	G21	MPIOB36	
MPIOB15 G18	IO_VREFB2N0_G18	IO_VREFB2N0_F21	F21	MPIOB37	
MPIOB16 E22	IO_VREFB2N0_E22	IO_VREFB2N1_G22	G22	MPIOB38	
MPIOB19 J16	IO_VREFB2N1_J16	IO_VREFB2N1_K22	K22	MPIOB39	
MPIOB20 E19	IO_VREFB2N0_E19	IO_VREFB2N0_F22	F22	MPIOB40	
MPIOB21 J17	IO_VREFB2N1_J17	IO_VREFB2N1_H21	H21	MPIOB41	
MPIOB22 H18	IO_VREFB2N0_H18	IO_VREFB2N1_K20	K20	MPIOB42	
MPIOB23 C21	IO_VREFB2N0_C21	IO_VREFB2N1_H22	H22	MPIOB43	
MPIOB3 G19	IO_VREFB2N0_G19	IO_VREFB2N1_J21	J21	MPIOB44	

U19E BANK5
EP2S15F484

MPIOB5 J8	IO_VREFB5N1_J8	IO_VREFB5N0_L8	L8	MPIOB17	
MPIOB6 L7	IO_VREFB5N0_L7	IO_VREFB5N1_J7	J7	MPIOB1	
K2	IO_VREFB5N0_K2	IO_VREFB5N1_H4	H4		
K1	IO_VREFB5N0_K1	IO_VREFB5N1_H3	H3		
K8	IO_VREFB5N0_K8	IO_VREFB5N1_G4	G4		
K7	IO_VREFB5N0_K7	IO_VREFB5N1_G3	G3		
K4	IO_VREFB5N0_K4	IO_VREFB5N1_F2	F2		
K3	IO_VREFB5N0_K3	IO_VREFB5N1_F1	F1		
K6	IO_VREFB5N0_K6	IO_VREFB5N1_G6	G6		TP31
K5	IO_VREFB5N0_K5	IO_VREFB5N1_G5	G5		
J3	IO_VREFB5N0_J3	IO_VREFB5N1_E2	E2		TP32
J2	IO_VREFB5N0_J2	IO_VREFB5N1_E1	E1		
J6	IO_VREFB5N0_J6	IO_VREFB5N1_F5	F5		TP33
J5	IO_VREFB5N0_J5	IO_VREFB5N1_F4	F4		
H2	IO_VREFB5N0_H2	IO_VREFB5N1_D2	D2		TP34
H1	IO_VREFB5N0_H1	IO_VREFB5N1_D1	D1		
H6	IO_VREFB5N0_H6	IO_VREFB5N1_E4	E4		TP35
H5	IO_VREFB5N0_H5	IO_VREFB5N1_E3	E3		
G2	IO_VREFB5N0_G2	IO_VREFB5N1_C2	C2		TP36
G1	IO_VREFB5N0_G1	IO_VREFB5N1_C1	C1		

SPARES IO

U19C BANK3
EP2S15F484

B15	IO_VREFB3N0_B15			
A15	IO_VREFB3N0_A15	IO_VREFB3N1_E14	E14	
C15	IO_VREFB3N0_C15	IO_VREFB3N1_G14	G14	
C16	IO_VREFB3N0_C16	IO_VREFB3N1_F14	F14	TP38
B16	IO_VREFB3N0_B16	IO_VREFB3N1_H14	H14	
A16	IO_VREFB3N0_A16	IO_VREFB3N1_D15	D15	TP39
F13	IO_VREFB3N0_F13	IO_VREFB3N1_F16	F16	
G13	IO_VREFB3N0_G13	IO_VREFB3N1_J15	J15	TP41
B17	IO_VREFB3N0_B17	IO_VREFB3N1_E15	E15	
A17	IO_VREFB3N0_A17	IO_VREFB3N1_F15	F15	TP42
A18	IO_VREFB3N0_A18	IO_VREFB3N1_G15	G15	
C17	IO_VREFB3N0_C17	IO_VREFB3N1_H16	H16	TP43
B18	IO_VREFB3N0_B18	IO_VREFB3N1_C19	C19	
C18	IO_VREFB3N0_C18	IO_VREFB3N1_D20	D20	TP44
C14	IO_VREFB3N0_C14	IO_VREFB3N1_G16	G16	
D14	IO_VREFB3N0_D14			

VCCIO3
R241 332R
D20 GREEN FPGA LED
RESET_SOFT_FPGA

U19D BANK4
EP2S15F484

FPGA_IO0 E6	IO_VREFB4N0_E6			
FPGA_IO1 D5	IO_VREFB4N0_D5	IO_VREFB4N1_B5	B5	
FPGA_IO2 H7	IO_VREFB4N0_H7	IO_VREFB4N1_A5	A5	FPGA_IO27
FPGA_IO3 C4	IO_VREFB4N0_C4	IO_VREFB4N1_C5	C5	FPGA_IO26
FPGA_IO4 D3	IO_VREFB4N0_D3	IO_VREFB4N1_C6	C6	FPGA_IO25
FPGA_IO5 E7	IO_VREFB4N0_E7	IO_VREFB4N1_B6	B6	FPGA_IO24
FPGA_IO6 G8	IO_VREFB4N0_G8	IO_VREFB4N1_A6	A6	FPGA_IO23
FPGA_IO7 D6	IO_VREFB4N0_D6	IO_VREFB4N1_E10	E10	FPGA_IO22
FPGA_IO8 F8	IO_VREFB4N0_F8	IO_VREFB4N1_B7	B7	FPGA_IO21
FPGA_IO9 F7	IO_VREFB4N0_F7	IO_VREFB4N1_A7	A7	FPGA_IO20
FPGA_IO10 D8	IO_VREFB4N0_D8	IO_VREFB4N1_C8	C8	FPGA_IO19
FPGA_IO11 E8	IO_VREFB4N0_E8	IO_VREFB4N1_C7	C7	FPGA_IO18
FPGA_IO12 F9	IO_VREFB4N0_F9	IO_VREFB4N1_B8	B8	FPGA_IO17
FPGA_IO13 E9	IO_VREFB4N0_E9	IO_VREFB4N1_A8	A8	FPGA_IO16
FPGA_IO14 G9	IO_VREFB4N0_G9			
FPGA_IO15 H9	IO_VREFB4N0_H9			

U19F BANK6
EP2S15F484

FPGA_IO28 W4	IO_VREFB6N0_W4			
FPGA_IO29 W3	IO_VREFB6N0_W3			
FPGA_IO30 Y2	IO_VREFB6N0_Y2	IO_VREFB6N1_R6	R6	TP37
FPGA_IO31 Y1	IO_VREFB6N0_Y1	IO_VREFB6N1_R5	R5	
FPGA_IO32 V4	IO_VREFB6N0_V4	IO_VREFB6N1_R4	R4	
FPGA_IO33 V3	IO_VREFB6N0_V3	IO_VREFB6N1_R3	R3	TP40
FPGA_IO34 W2	IO_VREFB6N0_W2	IO_VREFB6N1_P8	P8	
FPGA_IO35 W1	IO_VREFB6N0_W1	IO_VREFB6N1_P7	P7	
FPGA_IO36 R8	IO_VREFB6N0_R8	IO_VREFB6N1_T2	T2	FPGA_IO57
FPGA_IO37 R7	IO_VREFB6N0_R7	IO_VREFB6N1_T1	T1	FPGA_IO56
FPGA_IO38 V2	IO_VREFB6N0_V2	IO_VREFB6N1_P6	P6	FPGA_IO55
FPGA_IO39 V1	IO_VREFB6N0_V1	IO_VREFB6N1_P5	P5	FPGA_IO54
FPGA_IO40 U5	IO_VREFB6N0_U5	IO_VREFB6N1_R2	R2	FPGA_IO53
FPGA_IO41 U4	IO_VREFB6N0_U4	IO_VREFB6N1_R1	R1	FPGA_IO52
FPGA_IO42 T4	IO_VREFB6N0_T4	IO_VREFB6N1_N8	N8	FPGA_IO51
FPGA_IO43 T3	IO_VREFB6N0_T3	IO_VREFB6N1_N7	N7	FPGA_IO50
FPGA_IO44 T6	IO_VREFB6N0_T6	IO_VREFB6N1_P3	P3	FPGA_IO49
FPGA_IO45 T5	IO_VREFB6N0_T5	IO_VREFB6N1_P2	P2	FPGA_IO48
FPGA_IO46 U2	IO_VREFB6N0_U2			
FPGA_IO47 U1	IO_VREFB6N0_U1			

U19G BANK7
EP2S15F484

FPGA_IO58 AB8	IO_VREFB7N0_AB8	IO_VREFB7N1_V8	V8	FPGA_IO85
FPGA_IO59 AA8	IO_VREFB7N0_AA8	IO_VREFB7N1_V10	V10	FPGA_IO84
FPGA_IO60 Y8	IO_VREFB7N0_Y8	IO_VREFB7N1_R9	R9	FPGA_IO83
FPGA_IO61 Y7	IO_VREFB7N0_Y7	IO_VREFB7N1_T9	T9	FPGA_IO82
FPGA_IO62 AB7	IO_VREFB7N0_AB7	IO_VREFB7N1_U9	U9	FPGA_IO81
FPGA_IO63 AA7	IO_VREFB7N0_AA7	IO_VREFB7N1_T8	T8	FPGA_IO80
FPGA_IO64 T10	IO_VREFB7N0_T10	IO_VREFB7N1_U8	U8	FPGA_IO79
FPGA_IO65 U10	IO_VREFB7N0_U10	IO_VREFB7N1_V7	V7	FPGA_IO78
FPGA_IO66 AB6	IO_VREFB7N0_AB6	IO_VREFB7N1_W7	W7	FPGA_IO77
FPGA_IO67 AA6	IO_VREFB7N0_AA6	IO_VREFB7N1_U6	U6	FPGA_IO76
FPGA_IO68 Y6	IO_VREFB7N0_Y6	IO_VREFB7N1_AA4	AA4	FPGA_IO75
FPGA_IO69 Y5	IO_VREFB7N0_Y5	IO_VREFB7N1_Y3	Y3	FPGA_IO74
FPGA_IO70 AB5	IO_VREFB7N0_AB5	IO_VREFB7N1_T7	T7	FPGA_IO73
FPGA_IO71 AA5	IO_VREFB7N0_AA5	IO_VREFB7N1_V6	V6	FPGA_IO72

U19H BANK8
EP2S15F484

		IO_VREFB8N1_U13	U13	TP45
FPGA_IO86 R15	IO_VREFB8N0_R15	IO_VREFB8N1_V13	V13	
FPGA_IO87 Y20	IO_VREFB8N0_Y20	IO_VREFB8N1_Y18	Y18	TP46
FPGA_IO88 T15	IO_VREFB8N0_T15	IO_VREFB8N1_AA18	AA18	
V15	IO_VREFB8N0_V15	IO_VREFB8N1_Y17	Y17	TP47
FPGA_IO89 U15	IO_VREFB8N0_U15	IO_VREFB8N1_AB18	AB18	
FPGA_IO90 W15	IO_VREFB8N0_W15	IO_VREFB8N1_AB17	AB17	
FPGA_IO91 W16	IO_VREFB8N0_W16	IO_VREFB8N1_AA17	AA17	FPGA_IO95
U14	IO_VREFB8N0_U14	IO_VREFB8N1_T13	T13	
R14	IO_VREFB8N0_R14	IO_VREFB8N1_Y16	Y16	
TP48 V14	IO_VREFB8N0_V14	IO_VREFB8N1_AA16	AA16	
T14	IO_VREFB8N0_T14	IO_VREFB8N1_AB16	AB16	
Y14	IO_VREFB8N0_Y14	IO_VREFB8N1_Y15	Y15	
FPGA_IO92 W14	IO_VREFB8N0_W14	IO_VREFB8N1_AB15	AB15	FPGA_IO94
		IO_VREFB8N1_AA15	AA15	FPGA_IO93
		IO_VREFB8N1_W13	W13	
		IO_VREFB8N1_U12	U12	
		IO_VREFB8N1_Y13	Y13	

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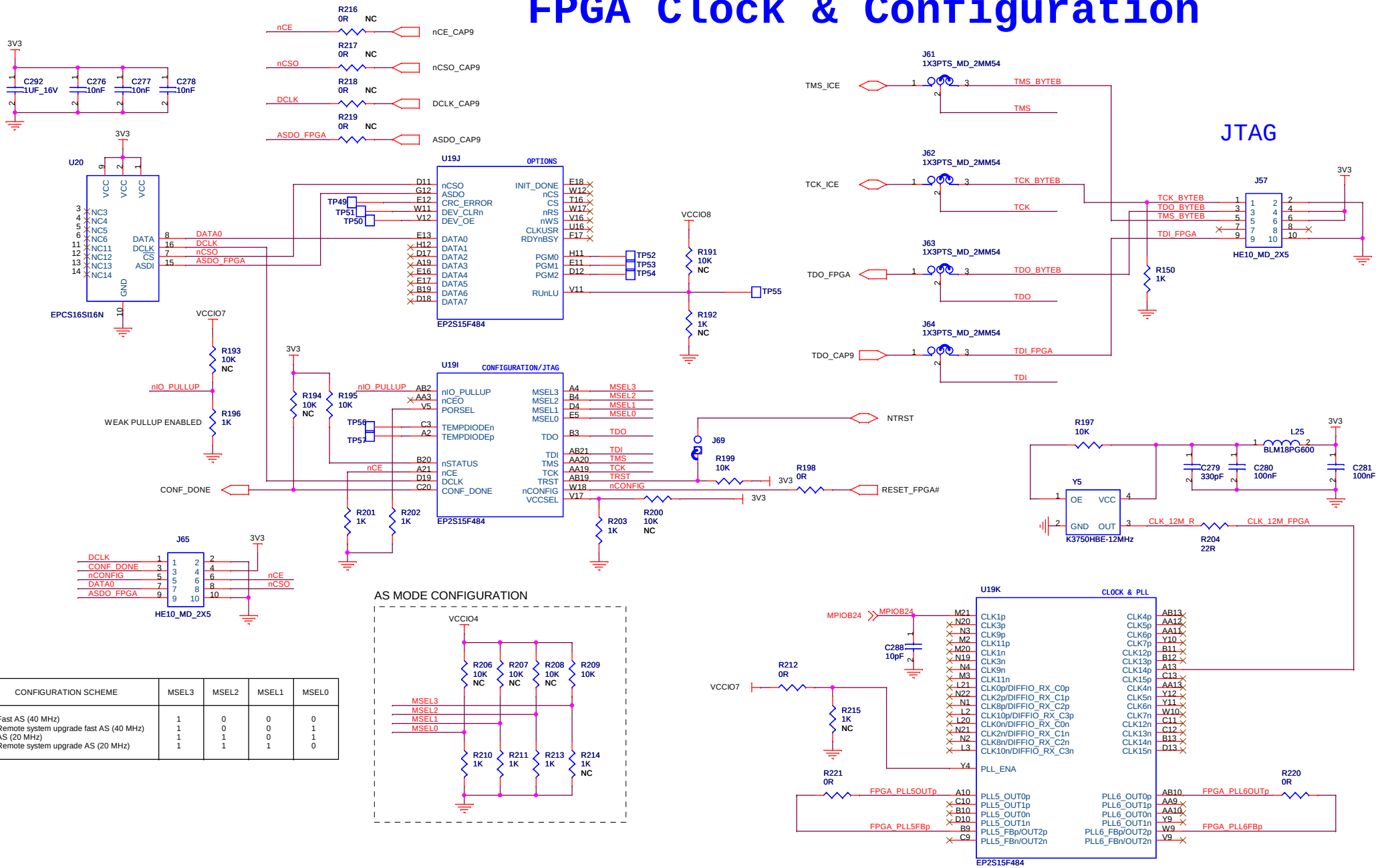
Projet / Project: CAP9-STK
Schéma électronique / Schematic: FPGA IO BANK

Rév.	Date	Auteur	Historique / Background history
C02	21/05/08	OBO	Création

Format: A3
Dessinateur / Drawer: O. Boitet
Référence / Reference: ADEC101389001
Rév.: C02
Date: Tuesday, May 20, 2008

FPGA Clock & Configuration



CONFIGURATION SCHEME	MSEL3	MSEL2	MSEL1	MSEL0
Fast AS (40 MHz)	1	0	0	0
Remote system upgrade fast AS (40 MHz)	1	0	0	1
AS (20 MHz)	1	0	1	1
Remote system upgrade AS (20 MHz)	1	1	1	0

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Rév.	Date	Auteur	Historique / Background history
C02	21/05/08	OBO	Création

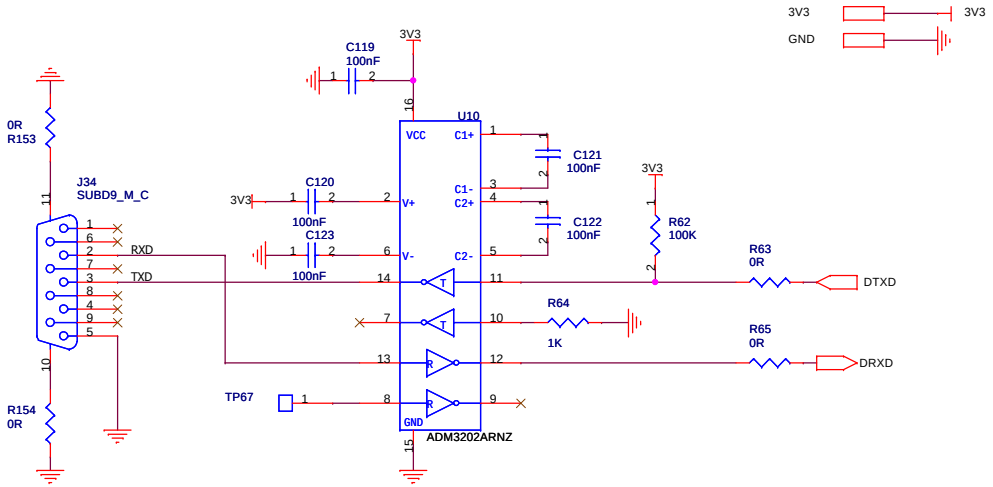
Projet / Project: CAP9-STK

Schéma électronique / Schematic: FPGA CLOCK & CONFIG

Format: A3 | Dessinateur / Drawer: O. Boitet | Référence / Reference: ADEC101389001 | Rév.: C02

Date: Tuesday, May 20, 2008 | Page 13 de / of 21

Serial Debug Port



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Rév.	Date	Auteur	Historique / Background history
C02	21/05/08	OBO	Création

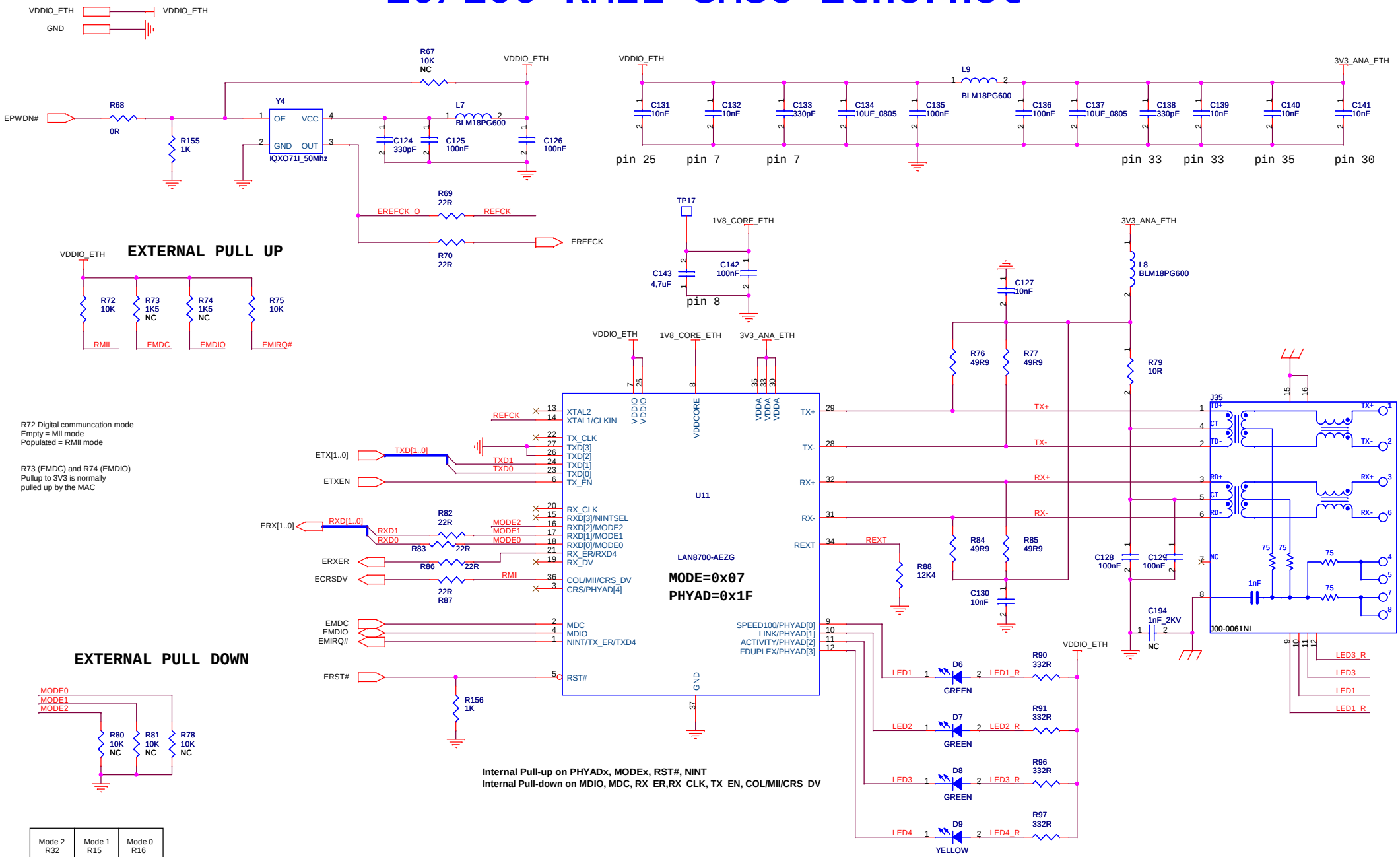
Projet / Project: CAP9-STK

Schéma électronique / Schematic: DEBUG

Format	Dessinateur / Drawer	Référence / Reference	Rév.
A3	O. Boitet	ADEC101389001	C02

Date: Tuesday, May 20, 2008

10/100 RMII SMSC Ethernet



Mode 2 R32	Mode 1 R15	Mode 0 R16		
Empty	Empty	Empty	111	All Capable [Default]
Empty	Empty	Populated	110	Power Down Mode
Empty	Populated	Empty	101	Repeater Mode
Empty	Populated	Populated	100	100Base-TX Half duplex Advertised
Populated	Empty	Empty	011	100Base-TX Full Duplex Auto Negotiate
Populated	Empty	Populated	010	100Base-TX Half Duplex Auto Negotiate
Populated	Populated	Empty	001	10Base-T Full Duplex Auto Negotiate
Populated	Populated	Populated	000	10Base-T Half Duplex Auto Negotiate

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C02	21/05/08	OBO	Création

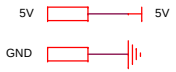
Projet / Project: CAP9-STK

Schéma électronique / Schematic: ETHERNET SMSC

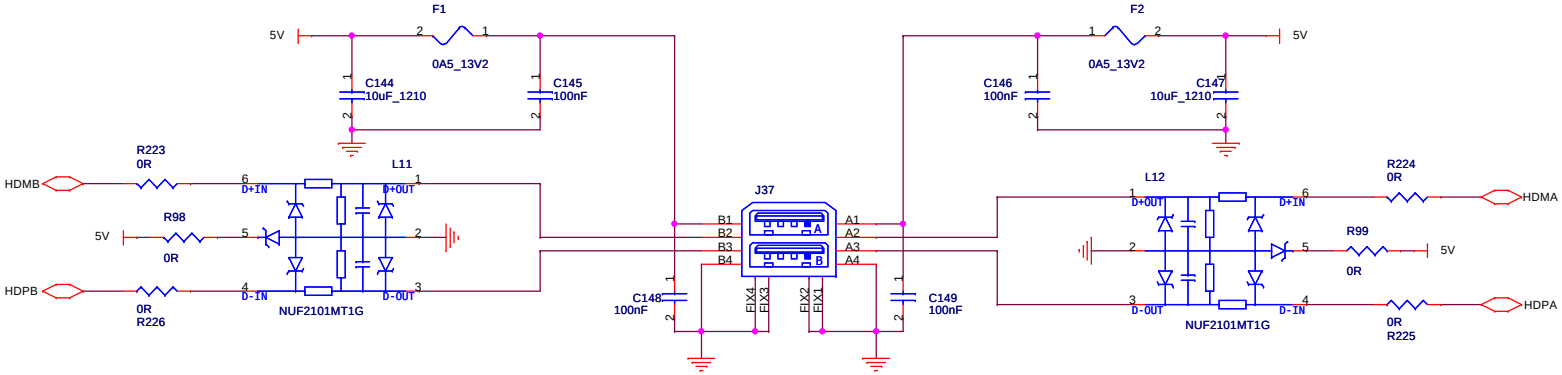
Format	Dessinateur / Drawer	Référence / Reference	Rév.
A3	O. Boitet	ADEC101389001	C02

Date: Tuesday, May 20, 2008

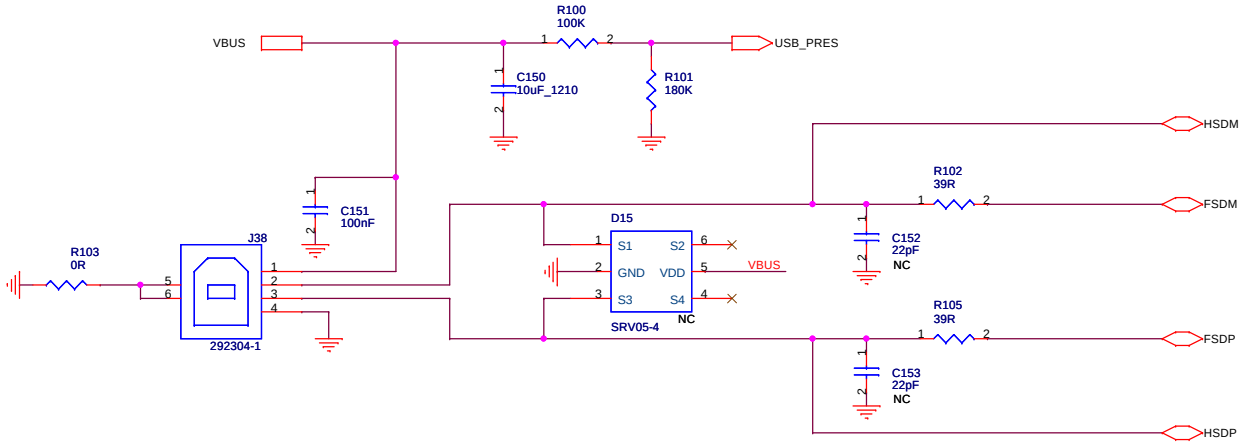
USB Interfaces



USB HOST INTERFACE



USB DEVICE INTERFACE



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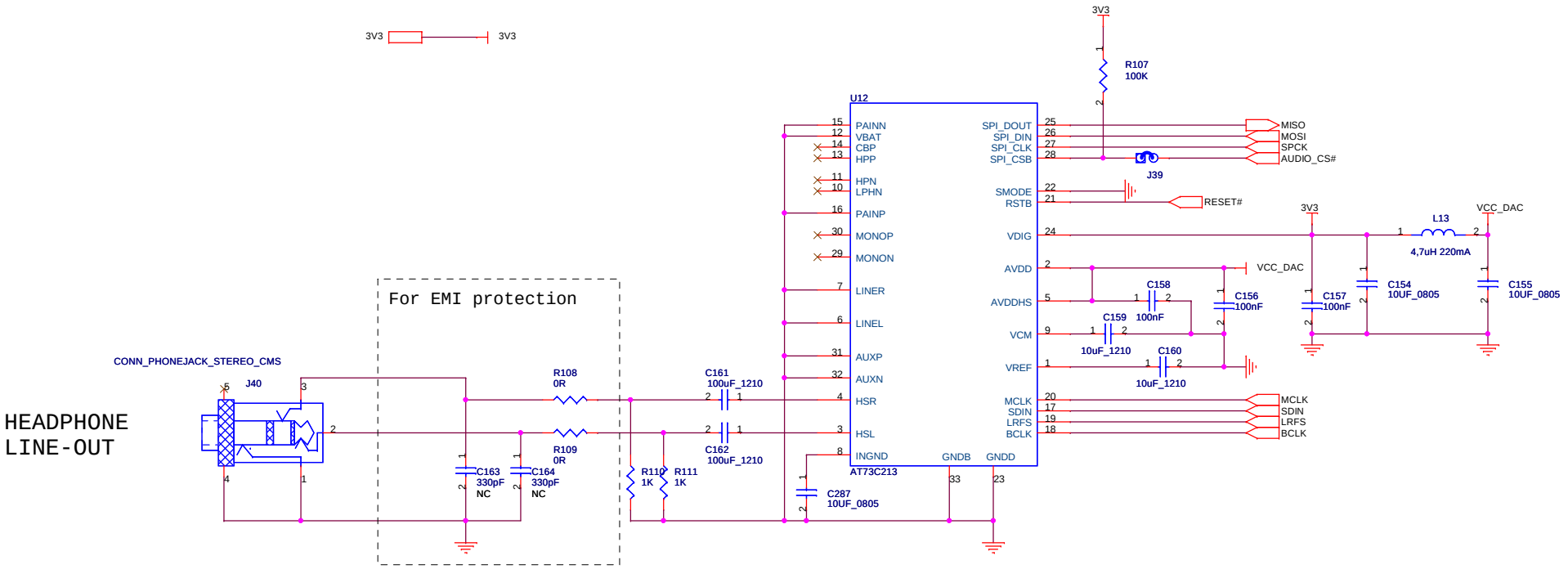
Rév.	Date	Auteur	Historique / Background history
C02	21/05/08	OBO	Création

Projet / Project	CAP9-STK
Schéma électronique / Schematic	USB HOST & DEVICE
Format	A3
Dessinateur / Drawer	O. Boitet
Référence / Reference	ADEC101389001
Rév.	C02
Date:	Tuesday, May 20, 2008
Page	16 de / of 21

Audio DAC



HEADPHONE
LINE-OUT

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Rév.	Date	Auteur	Historique / Background history
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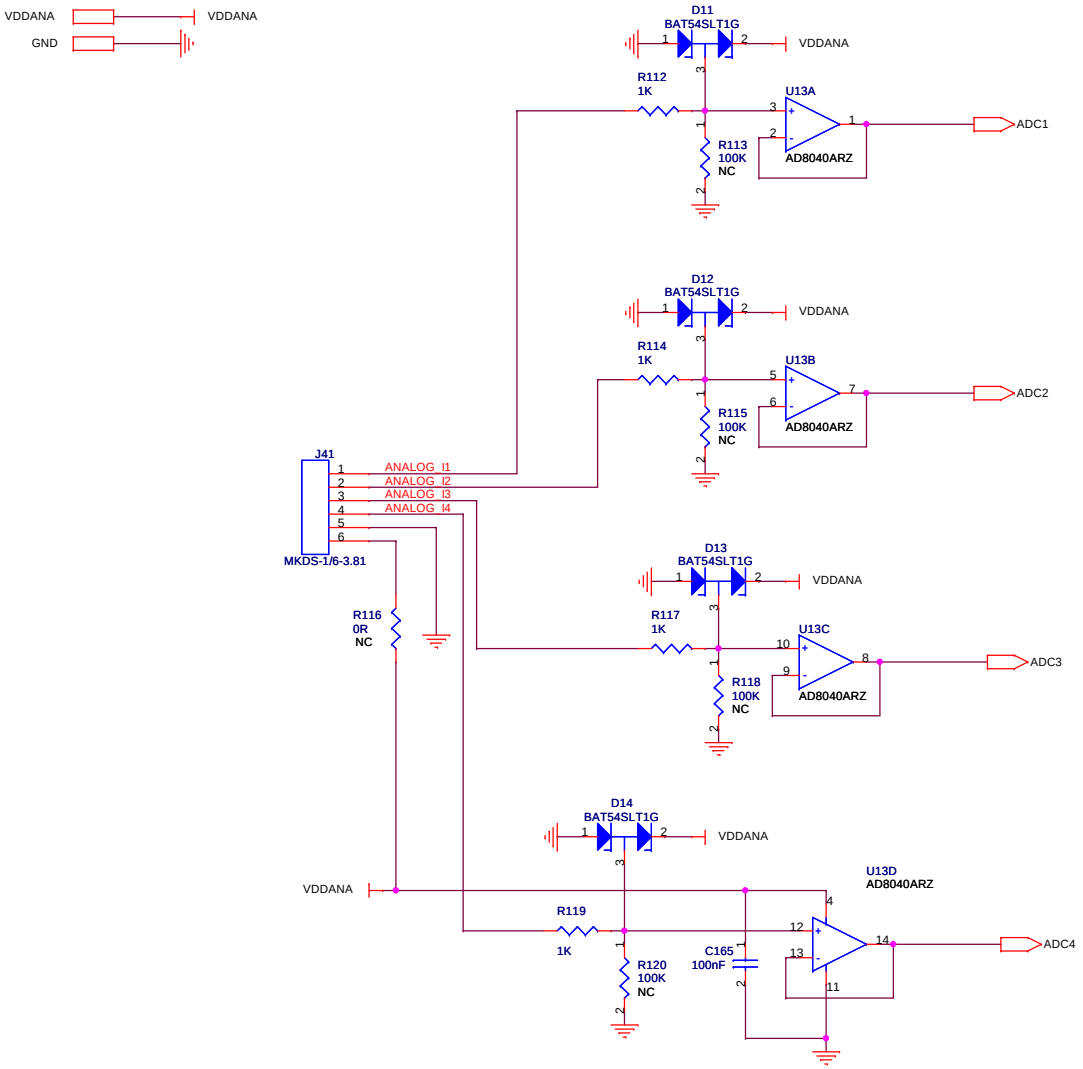
Projet / Project: CAP9-STK

Schéma électronique / Schematic: AUDIO

Format	Dessinateur / Drawer	Référence / Reference	Rév.
A3	O. Boitet	ADEC101389001	C02

Date: Tuesday, May 20, 2008

Analog Inputs



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Rév.	Date	Auteur	Historique / Background history
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Projet / Project: CAP9-STK

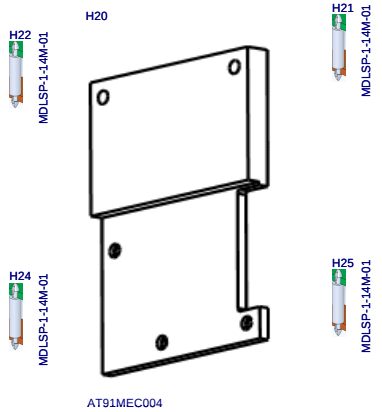
Schéma électronique / Schematic: ANALOG

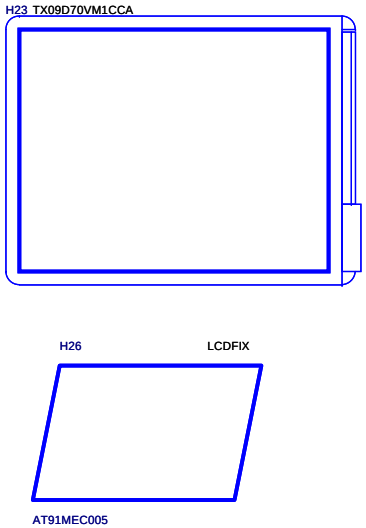
Format	Dessinateur / Drawer	Référence / Reference	Rév.
A3	O. Boitet	ADEC101389001	C02

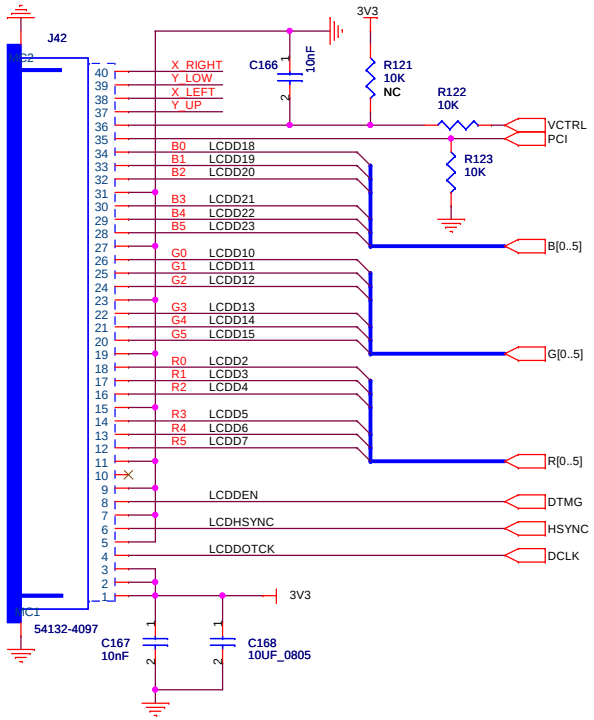
Date: Tuesday, May 20, 2008

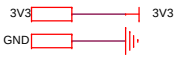
LCD Connector & Touch Screen Controller

3.5-inch 1/4 VGA TFT LCD DISPLAY

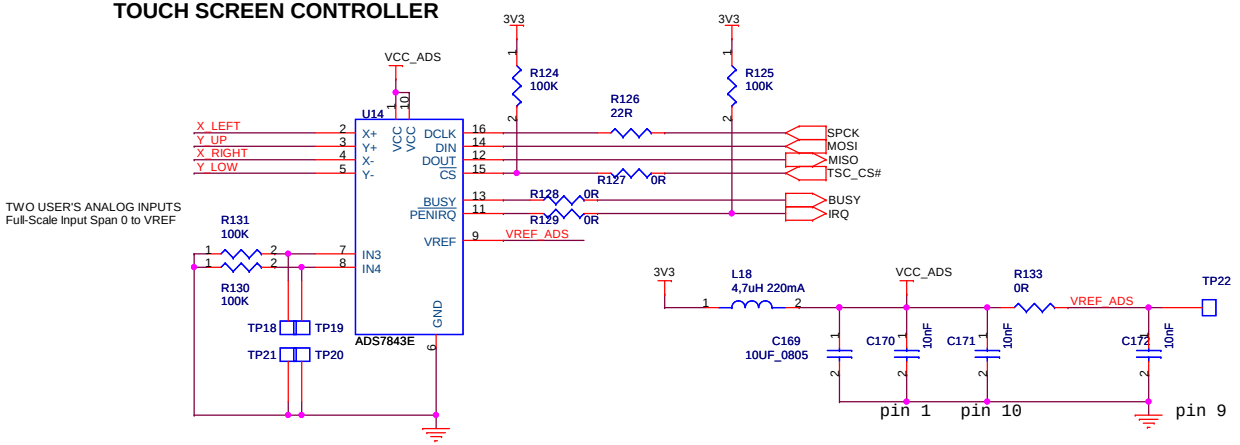








TOUCH SCREEN CONTROLLER



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Rév.	Date	Auteur	Historique / Background history
C02	21/05/08	OBO	Création

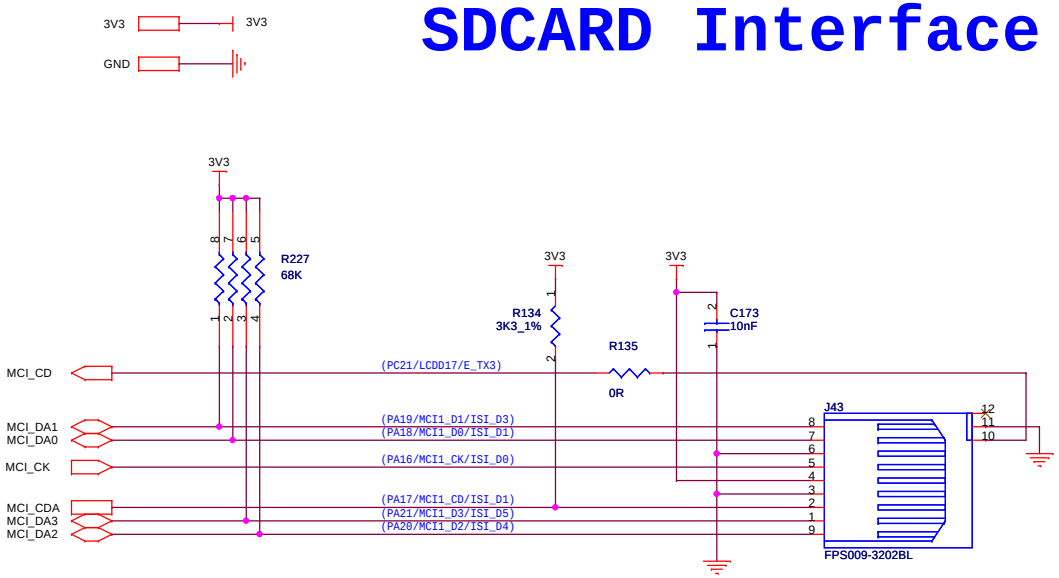
Projet / Project: CAP9-STK

Schéma électronique / Schematic: LCD & TSC

Format	Dessinateur / Drawer	Référence / Reference	Rév.
A3	O. Boitet	ADEC101389001	C02

Date: Tuesday, May 20, 2008

SDCARD Interface



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Rév.	Date	Auteur	Historique / Background history
C02	21/05/08	OBO	Création

Projet / Project: CAP9-STK

Schéma électronique / Schematic: SDCARD

Format: A3

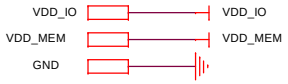
Dessinateur / Drawer: O. Boitet

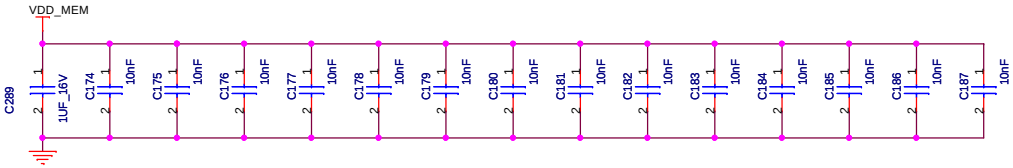
Référence / Reference: ADEC101389001

Rév.: C02

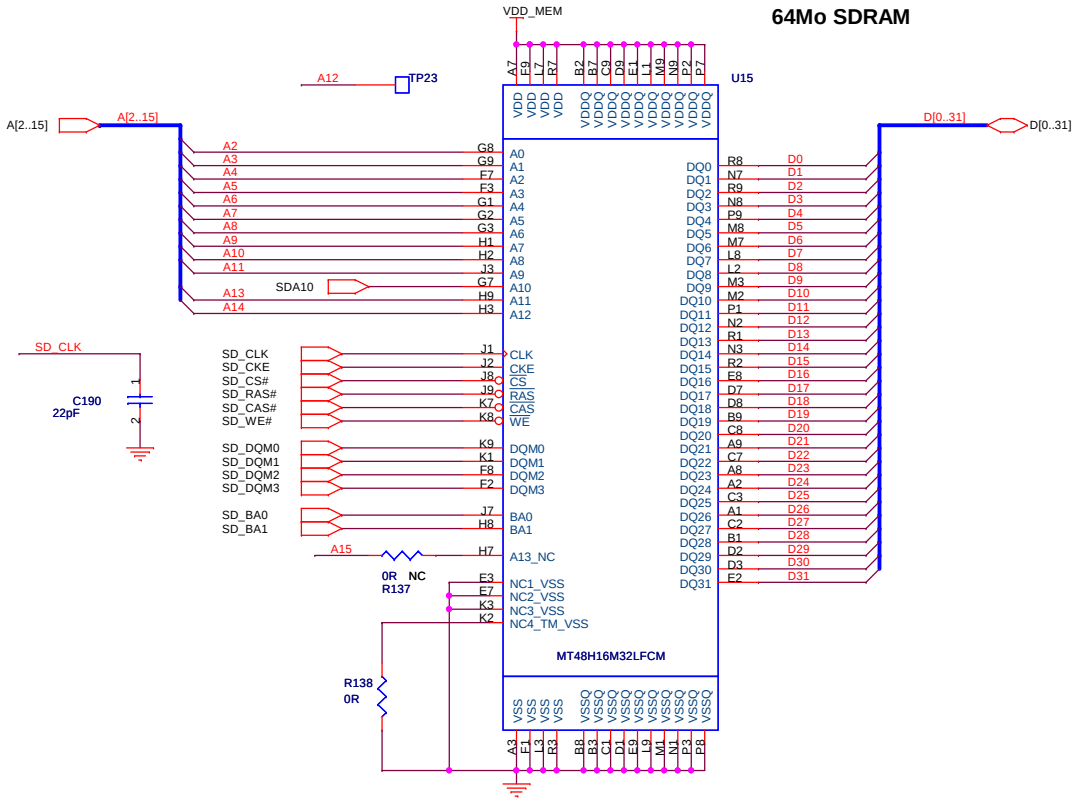
Date: Tuesday, May 20, 2008

SDRAM & Flash Memories

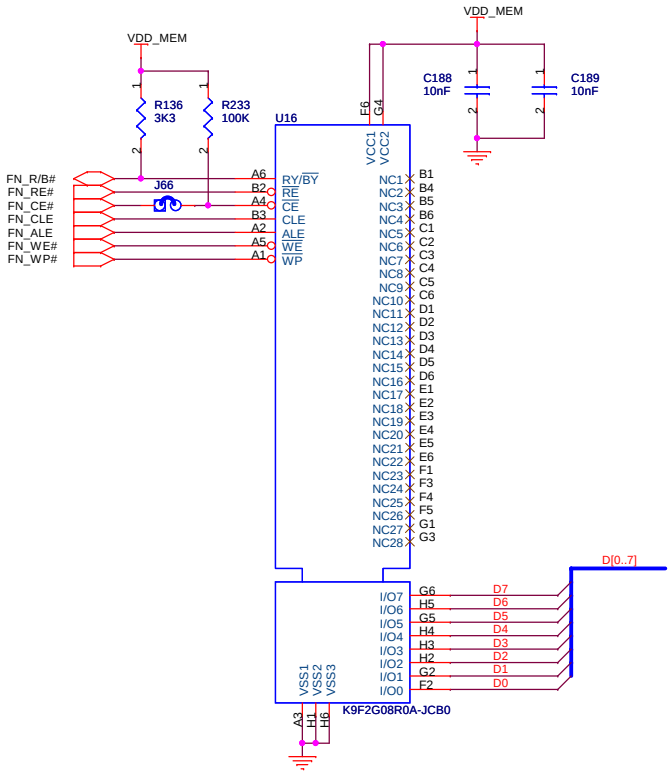




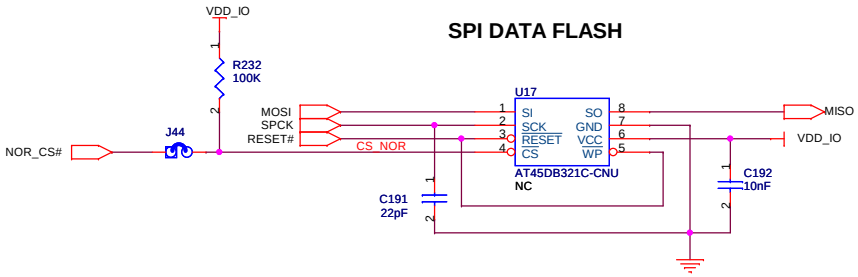
64Mo SDRAM



2Gb NAND FLASH



SPI DATA FLASH



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Projet / Project: CAP9-STK

Schéma électronique / Schematic: SDRAM, NAND & DATAFLASH

Format	Dessinateur / Drawer	Référence / Reference	Rév.
A3	O. Boitet	ADEC101389001	C02

Date: Tuesday, May 20, 2008

Section 5

Revision History

5.1 Revision Hisory

Document	Comments	Change Request Ref
6351A	First Issue	
6351B	Section ”AT91CAP9-STK Schematics” on page 4-1 updated Section 1.2 on page 1-1, removed ‘”A” from AT91CAP9-STK	5606

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