AK4954A

32-bit Stereo CODEC with MIC/HP/SPK-AMP

GENERAL DESCRIPTION

The AK4954A is a low power consumption 32-bit stereo CODEC with a microphone, a headphone and a speaker amplifiers. The input circuits include a microphone amplifier and an ALC (Automatic Level Control) circuit, and the output circuits include a cap-less headphone amplifier and a speaker amplifier. It is suitable for portable application with recording/playback function. The integrated charge pump circuit generates a negative voltage and removes the output AC coupling capacitors. The speaker amplifier has a wide operating voltage range, which is from 0.9V to 5.5V, enabling a direct drive to batteries. The AK4954A is available in a small 32-pin QFN (4x4mm 0.4mm pitch), utilizing less board space than competitive offerings.

FEATURES

1. Recording Function
- **Two Low Noise Microphone Power Supplies**
- **Stereo Single-ended input with three Selectors**
- **Low Noise Microphone Amplifier (+26dB/+20dB/+13dB/+6dB/0dB)**
- **Digital ALC (Automatic Level Control)**
  (Setting Range: +36dB ~ –52.5dB, 0.375dB Step)
- **ADC Performance: S/(N+D): 88dB, DR, S/N: 97dB (Microphone Amplifier =+20dB)**
  S/(N+D): 88dB, DR, S/N: 100dB (Microphone Amplifier =0dB)
- **Two Types of Decimation Filters**
- **Overflow Detection**
- **Wind-noise Reduction Filter**
- **Stereo Separation Emphasis Circuit**
- **5-band Notch Filter**
- **Digital Microphone Interface**

2. Playback Function
- **Digital ALC (Automatic Level Control)**
  (Setting Range: +36dB ~ –52.5dB, 0.375dB Step)
- **3-band Dynamic Range Control Circuit**
- **Digital Volume Control (+6dB ~ –65.5dB, 0.5dB Step, Mute)**
- **Capacitor-less Stereo Headphone Amplifier**
  - **HP-Amplifier Performance: S/(N+D): 65dB@20mW, S/N: 100dB**
  - **Output Power: 20mW@16Ω**
  - **Pop Noise Free at Power-ON/OFF**
- **Mono Speaker-Amplifier (with Stereo Line Output Switch)**
  - **SPK-Amplifier Performance: S/(N+D): 70dB@250mW**
    Output Noise Level: -97dBV
  - **BTL Output**
  - **Output Power: 400mW@8Ω (SVDD=3.3V)**
    100mW@8Ω (SVDD=1.5V)
- **Beep Generator**

3. Power Management

4. Master Clock:
(1) PLL Mode
- **Frequencies: 11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)**
  32fs or 64fs (BICK pin)

(2) External Clock Mode
- **Frequencies: 256fs, 384fs, 512fs or 1024fs (MCKI pin)**

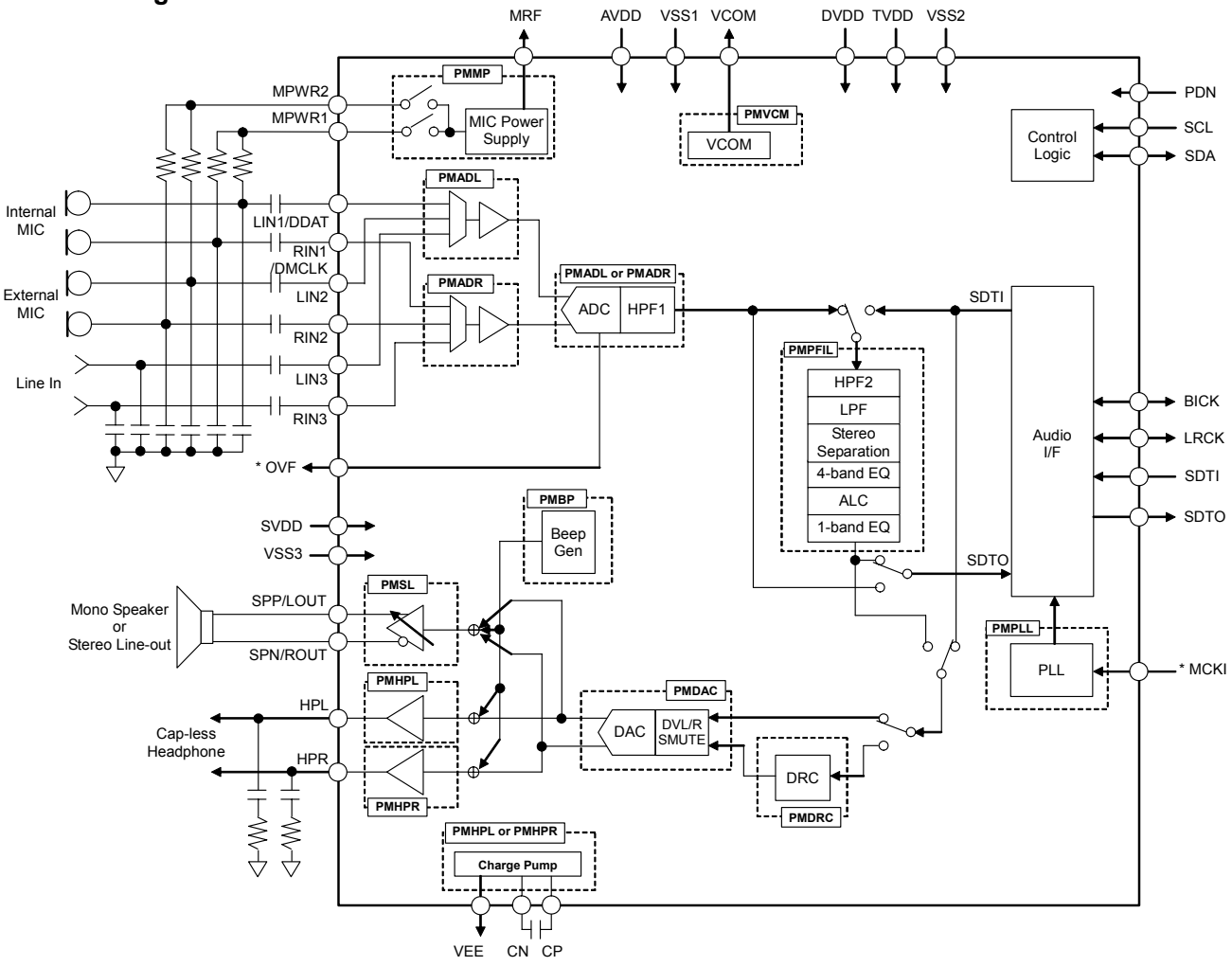
5. Sampling Frequencies
- **PLL Slave Mode (BICK pin): 8kHz ~ 96kHz**
- **PLL Master Mode: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz**
- **EXT Master/Slave Mode: 8kHz ~ 96kHz (256fs), 8kHz ~ 48kHz (384fs), 8kHz ~ 48kHz (512fs), 8kHz ~ 12kHz (1024fs)**

6. Master/Slave mode
7. Audio Interface Format: MSB First, 2's complement
- **ADC: 16/24/32-bit MSB justified, 16/24/32-bit I^{2}S**
- **DAC: 16/24/32-bit MSB justified, 16/24-bit LSB justified, 16/24/32-bit I^{2}S**

8. Serial μP I/F: I^{2}C Bus (Ver 1.0, 400kHz Fast-Mode)
9. Ta = –30 ~ 85°C
10. Power Supply:
- **Analog Power Supply (AVDD): 2.5 ~ 3.5V**
- **Digital Power Supply (DVDD): 1.6 ~ 1.98V**
- **Digital I/O Power Supply (TVDD): 1.6 or (DVDD-0.2) ~ 3.5V**
- **Speaker Power Supply (SVDD): 0.9 ~ 5.5V**

11. Package: 32-pin QFN (4 x 4mm, 0.4mm pitch)

■ Block Diagram

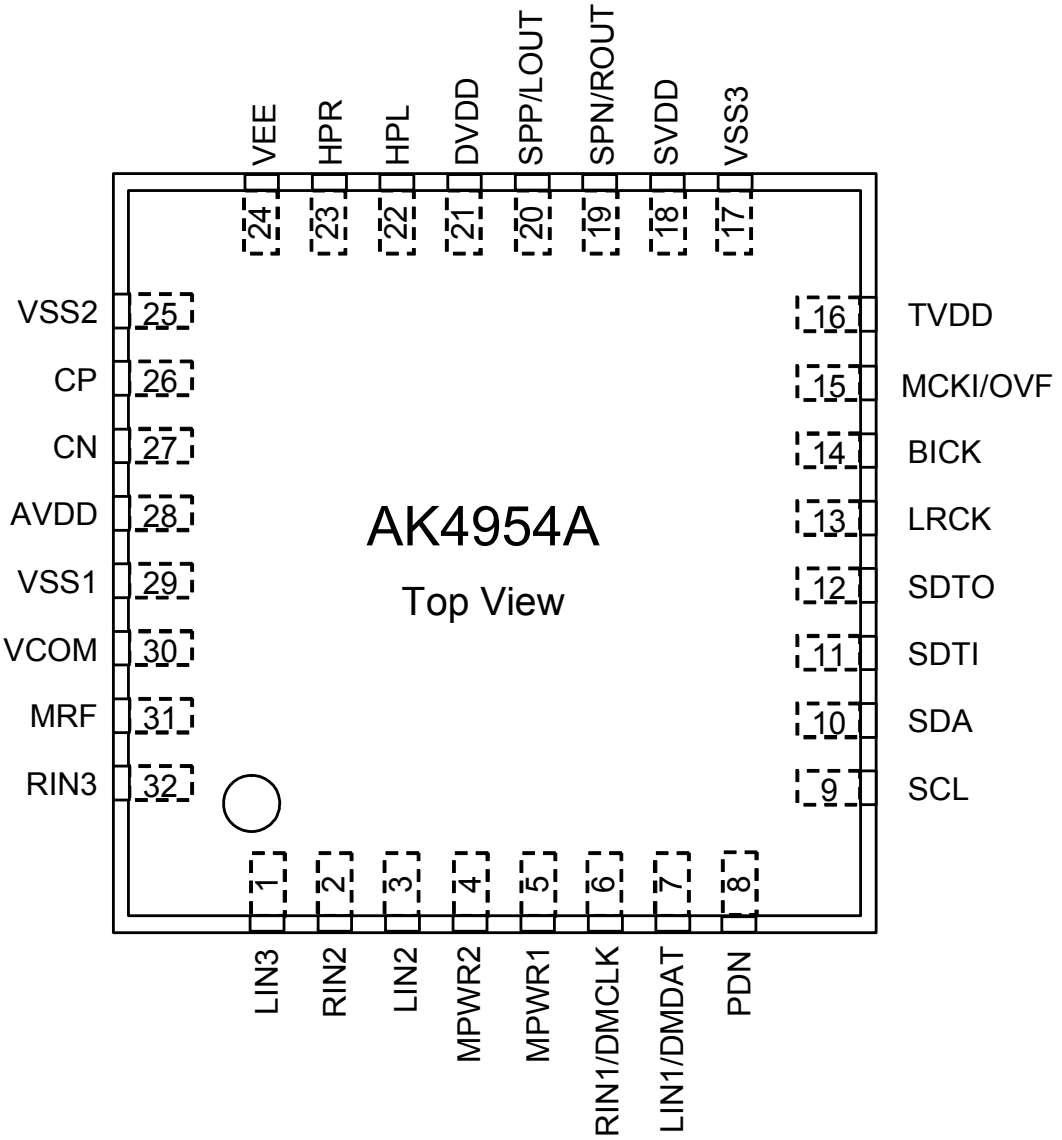


(The OVF and MCKI pins share the No. 15 pin terminal.)
Figure 1. Block Diagram

■ Ordering Guide

AK4954AEN	–30 ~ +85°C	32-pin QFN (0.4mm pitch)
AKD4954	Evaluation board for AK4954A	

■ Pin Layout



■ Comparison with AK4953A

Function	AK4953A	AK4954A
Resolution	24-bit	32-bit
AVDD	2.85V ~ 3.5V	2.5V ~ 3.5V
DVDD	1.6V ~ 2.0V	1.6V ~ 1.98V
SVDD	0.9V ~ 5.5V	←
TVDD	DVDD ~ 3.5V	1.6V or (DVDD-0.2)V ~ 3.5V
ADC DR, S/N	88dB @ MGAIN = +20dB 96dB @ MGAIN = 0dB	97dB @ MGAIN = +20dB 100dB @ MGAIN = 0dB
DAC S/N	96dB	100dB
Input level	typ. 2.4Vpp @ MIC Gain=0dB	typ. 0.8 x AVDD @ MGAIN=0dB
Output level (Headphone)	typ. 1.75Vpp @ DVOL=0dB	typ. 0.485 x AVDD @ DVOL=0dB
MIC Power Output Voltage	typ 2.3V (2 Line Outputs)	0.8 x AVDD (2 Line Outputs)
MIC Power Output Noise	-108dBV (A-weighted)	-120dBV (A-weighted)
MIC-Amp	0dB/+12dB/+16dB/+20dB/+23dB/ +26dB/+29dB	0dB/+6dB/+13dB/+20dB/+26dB
ADC Overflow Output	No	Yes (pin selectable OVF/MCKI)
Stereo Emphasis	No	Yes
Output Volume	+36dB ~ -54dB, 0.375dB Step (Note 1) & +12dB ~ -115dB, 0.5dB Step	+36dB ~ -52.5dB, 0.375dB Step (Note 1) & +6dB ~ -65.5dB, 0.5dB Step
Dynamic Range Control	No	Yes (for Playback)
Line Output Switch for Speaker-Amp	No	Yes
Master Clock Reference for PLL Mode	11.2896MHz, 12MHz, 13.5MHz, 24MHz, 27MHz	11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz
Serial µP Interface	3-wire Serial or I^2C Bus	I^2C Bus
Power Consumption **(Stereo Recording)** **(Headphone Playback)**	 typ. 9.4mW typ. 10.2mW	 typ. 10.4mW (Low-power operation mode) typ. 6.2mW (Low-power operation mode)
Package	36-pin QFN (5 x 5mm, 0.4mm pitch)	32-pin QFN (4 x 4mm, 0.4mm pitch)

Note 1. ALC and Volume circuits are shared by input and output. Therefore, it is impossible to use ALC and Volume control function at the same time for both recording and playback mode.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LIN3	I	Lch Analog Input 3 Pin
2	RIN2	I	Rch Analog Input 2 Pin
3	LIN2	I	Lch Analog Input 2 pin
4	MPWR2	O	Microphone Power Supply Pin for Microphone 2
5	MPWR1	O	Microphone Power Supply Pin for Microphone 1
6	RIN1	I	Rch Analog Input 1 Pin (DMIC bit = "0": default)
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")
7	LIN1	I	Lch Analog Input 1 Pin (DMIC bit = "0": default)
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
8	PDN	I	Power-down & Reset When "L", the AK4954A is in power-down mode and is held in reset. The AK4954A must be always reset upon power-up.
9	SCL	I	Control Data Clock Pin
10	SDA	I/O	Control Data Input/Output Pin
11	SDTI	I	Audio Serial Data Input Pin
12	SDTO	O	Audio Serial Data Output Pin
13	LRCK	I/O	Input/Output Channel Clock Pin
14	BICK	I/O	Audio Serial Data Clock Pin
15	MCKI	I	External Master Clock Input Pin (OVFL bit = "0": default)
	OVF	O	Over Flow Flag Output Pin (OVFL bit = "1")
16	TVDD	-	Digital I/O Power Supply Pin, 1.6 ~ 3.5V
17	VSS3	-	Ground 3 Pin
18	SVDD	-	Speaker Amplifier Power Supply Pin, 0.9 ~ 5.5V
19	SPN	O	Speaker Amplifier Negative Output Pin (LOSEL bit = "0": default)
	ROUT	O	Rch Stereo Line Output Pin (LOSEL bit = "1")
20	SPP	O	Speaker Amplifier Positive Output Pin (LOSEL bit = "0": default)
	LOUT	O	Lch Stereo Line Output Pin (LOSEL bit = "1")
21	DVDD	-	Digital Power Supply Pin, 1.6 ~1.98V
22	HPL	O	Lch Headphone Amplifier Output Pin
23	HPR	O	Rch Headphone Amplifier Output Pin
24	VEE	O	Charge-Pump Circuit Negative Voltage Output Pin This pin must be connected to VSS2 with 2.2µF±50% capacitor in series.
25	VSS2	-	Ground 2 Pin
26	CP	O	Positive Charge-Pump Capacitor Terminal Pin This pin must be connected to CN pin with 2.2µF±50% capacitor in series.
27	CN	I	Negative Charge-Pump Capacitor Terminal Pin This pin must be connected to CP pin with 2.2µF±50% capacitor in series.
27	AVDD	-	Analog Power Supply Pin, 2.5 ~ 3.5V
29	VSS1	-	Ground 1 Pin
30	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 with 2.2µF±50% capacitor in series.
31	MRF	O	Microphone Power Supply Ripple Filter Pin This pin must be connected to VSS1 with 2.2µF±50% capacitor in series.
32	RIN3	I	Rch Analog Input 3 Pin

Note 2. All input pins except analog input pins (LIN1, RIN1, LIN2, RIN2, LIN3, RIN3) must not be allowed to float.

■ Handling of Unused Pin

The unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	MPWR1, MPWR2, MRF, SPN, SPP, HPL, HPR, CP, CN, VEE, LIN1/DMDAT, RIN1/DMCLK, LIN2, RIN2, LIN3, RIN3	Open.
Digital	MCKI/OVF	Connect to VSS2 and set OVFL bit = "0".
	SDTI	Connect to VSS2
	SDTO	Open

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=0V; Note 3)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	2.5	V
	Digital I/O	TVDD	–0.3	6.0	V
	Speaker Amplifier	SVDD	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 5)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 6)		VIND	–0.3	TVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 7)		Pd	-	900	mW

Note 3. All voltages are with respect to ground.

Note 4. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.

Note 5. LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins

Note 6. PDN, SCL, SDA, SDTI, LRCK, BICK and MCKI pins
Pull-up resistors at SDA and SCL pins should be connected to (TVDD+0.3)V or less voltage.

Note 7. This power is the AK4954A internal dissipation that does not include power dissipation of externally connected speakers. The maximum junction temperature is 125°C and θja (Junction to Ambient) is 42°C/W at JESD51-9 (2p2s). When Pd =900mW and the θja is 42°C/W, the junction temperature does not exceed 125°C. In this case, there is no case that the AK4954A is damaged by its internal power dissipation. Therefore, the AK4954A should be used in the condition of θja ≤ 42°C/W.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3= 0V; Note 3)

Parameter		Symbol	min	typ	max	Unit
Power Supplies	Analog	AVDD	2.5	3.3	3.5	V
(Note 8)	Digital	DVDD	1.6	1.8	1.98	V
	Digital I/O (Note 9)	TVDD	1.6 or (DVDD-0.2)	1.8	3.5	V
	SPK Amplifier	SVDD	0.9	3.3	5.5	V

Note 3. All voltages are with respect to ground.

Note 8. The power-up sequence between AVDD, DVDD, TVDD and SVDD is not critical. The PDN pin must be "L" upon power-up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

Note 9. The minimum value is higher voltage between DVDD-0.2V and 1.6V.

*** When SVDD is powered ON and the PDN pin is "L", AVDD, DVDD or TVDD can be powered ON/OFF. When TVDD is powered ON and the PDN pin is "L", AVDD, DVDD or SVDD can be powered ON/OFF. The PDN pin must be set to "H" after all power supplies are ON when the AK4954A is powered-up from power-down state.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=SVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=VSS3=0V; fs=44.1kHz, BICK=64fs; Signal Frequency=1kHz; 24-bit Data; Measurement Bandwidth=20Hz ~ 20kHz; unless otherwise specified)

Parameter			min	typ	max	Unit
Microphone Amplifier: LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins						
Input Resistance			70	100	140	kΩ
Gain	MGAIN2-0 bits = "000"		+5	+6	+7	dB
	MGAIN2-0 bits = "001"		+12	+13	+14	dB
	MGAIN2-0 bits = "010"		+19	+20	+21	dB
	MGAIN2-0 bits = "011"		+25	+26	+27	dB
	MGAIN2-0 bits = "1xx"		-	0	-	dB
Microphone Power Supply: MPWR1, MPWR2 pins						
Output Voltage (Note 10)			2.51	2.64	2.77	V
Output Noise Level (A-weighted)			-	-120	-	dBV
PSRR (fin = 1kHz) (Note 11)			-	70	-	dB
Load Resistance			1.0	-	-	kΩ
Load Capacitance			-	-	15	pF
ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3 pins → ADC → Programmable Filter (IVOL=0dB, EQ=ALC=OFF) → SDTO; C_{ext1} = 1µF, C_{ext2} = 1nF (Note 12)						
Resolution			-	-	32	Bits
Input Voltage (Note 13)		(Note 14)	0.237	0.264	0.29	Vpp
		(Note 15)	2.37	2.64	2.90	Vpp
S/(N+D) (–1dBFS)	fs=44.1kHz BW=20kHz	(Note 14)	78	88	-	dBFS
		(Note 15)	-	88	-	dBFS
	fs=96kHz BW=40kHz	(Note 14)	-	85	-	dBFS
		(Note 15)	-	82	-	dBFS
D-Range (–60dBFS, A-weighted)		(Note 14)	87	97	-	dB
		(Note 15)	-	100	-	dB
S/N (A-weighted)		(Note 14)	87	97	-	dB
		(Note 15)	-	100	-	dB
Interchannel Isolation		(Note 14)	80	100	-	dB
		(Note 15)	-	100	-	dB
Interchannel Gain Mismatch		(Note 14)	-	0	0.8	dB
		(Note 15)	-	0	0.5	dB
PSRR (fin = 1kHz) (Note 11, Note 14)			-	40	-	dB

Note 10. The output voltage is proportional to AVDD. (typ. 0.8 x AVDD V)
Note 11. PSRR is applied to AVDD with 100mpVpp sine wave.
Note 12. Measured by the circuit shown below (Figure 2). (C_{ext2} can also be placed between the input pin and VSS1.)

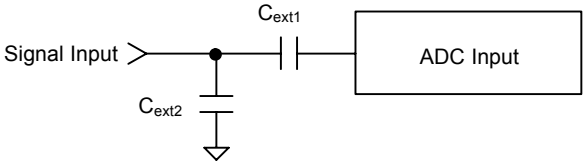


Figure 2. ADC Analog Characteristics Measurement Circuit

Note 13. The input voltage is proportional to AVDD.
typ. 0.8 x AVDD Vpp (0dB), typ. 0.08 x AVDD Vpp (+20dB)
Note 14. MGAIN2-0 bits = "010" (+20dB)
Note 15. MGAIN2-0 bits = "1xx" (0dB).

Parameter			min	typ	max	Unit
DAC Characteristics:						
Resolution			-	-	32	Bits
Headphone Amplifier Characteristics: DAC → HPL, HPR pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=16Ω						
Output Voltage (Note 16)			1.44	1.60	1.76	Vpp
S/(N+D)	(R_L=16Ω)	fs=44.1kHz, BW=20kHz	55	65	-	dB
		fs=96kHz, BW=40kHz	-	65	-	dB
	(R_L=10kΩ)	fs=44.1kHz, BW=20kHz	-	80	-	dB
S/N (A-weighted)			90	100	-	dB
Interchannel Isolation			65	80	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Output Offset Voltage			- 1	0	+ 1	mV
PSRR (fin = 1kHz) (Note 17)			-	40	-	dB
Load Resistance			16	-	-	Ω
Load Capacitance			-	-	300	pF
Speaker Amplifier Characteristics: DAC → SPP/SPN pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=8Ω, BTL						
Output Voltage						
SLG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	3.18	-	Vpp
SLG1-0 bits = "01", –0.5dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SLG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	1.79	-	Vrms
SLG1-0 bits = "00", –1.5dBFS (Po=100mW) (Note 18)			-	0.9	-	Vrms
S/(N+D)						
SLG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	70	-	dB
SLG1-0 bits = "01", –0.5dBFS (Po=250mW)			40	70	-	dB
SLG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	20	-	dB
SLG1-0 bits = "00", –1.5dBFS (Po=100mW) (Note 18)			-	20	-	dB
Output Noise Level (A-weighted, SLG1-0 bits = "01")			-	-97	-87	dBV
Output Offset Voltage			-30	0	+30	mV
PSRR (fin = 1kHz) (Note 19)			-	50	-	dB
Load Resistance			6.8	8	-	Ω
Load Capacitance			-	-	30	pF
Stereo Line Output Characteristics: DAC → LOUT, ROUT pins, ALC=OFF, IVOL=DVOL=SLG= 0dB, R_L=10kΩ						
Output Voltage (Note 20)			-	2.24	-	Vpp
S/(N+D)			74	84	-	dB
S/N (A-weighted)			84	94	-	dB
Interchannel Isolation			-	90	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Load Resistance			10	-	-	kΩ
Load Capacitance			-	-	30	pF

Note 16. The full-scale output voltage is proportional to AVDD. (typ. 0.485 x AVDD Vpp)
Note 17. PSRR is applied to AVDD or DVDD with 100mpVpp sine wave.
Note 18. When SVDD = 1.5V.
Note 19. PSRR is applied to AVDD or SVDD with 100mpVpp sine wave.
Note 20. The full-scale output voltage is proportional to AVDD. (typ. 0.68 x AVDD Vpp)

Parameter			min	typ	max	Unit
Beep Output Characteristics: BEEP Generator → HPL, HPR pins, SPP/SPN pins, LOUT, ROUT pins						
Output Voltage (BPLVL = 0dB)						
	HPL, HPR pins (R_L=16Ω)		-	1.5	-	Vpp
	SPP/SPN pins (R_L=8Ω, BTL, SLG = +4.26dB)		-	2.8	-	Vpp
	LOUT, ROUT pins (R_L=10kΩ, SLG = 0dB)		-	1.4	-	Vpp
Gain						
	Gain Setting		-60	-	0	dB
	Step Width		-	3	-	dB
Power Supplies:						
Power-up (PDN pin = "H")						
	MIC + ADC + DAC + Headphone out					
		AVDD+DVDD+TVDD (Note 21)	-	9.2	13.8	mA
		AVDD+DVDD+TVDD (Note 22)	-	8.2	-	mA
		SVDD (No Load)	-	8	12	μA
	MIC + ADC + DAC + Speaker out					
		AVDD+DVDD+TVDD (Note 23)	-	8.2	12.3	mA
		AVDD+DVDD+TVDD (Note 24)	-	7.2	-	mA
		SVDD (No Load)	-	0.8	1.2	mA
Power-down (PDN pin = "L") (Note 25)						
	AVDD+DVDD+TVDD+SVDD		-	0	10	μA
	SVDD (Note 26)		-	0	10	μA

Note 21. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMHPL=PMHPR= PMVCM=PMPLL=PMBP=PMMP=M/S bits = "1", and LPMIC = LPDA bits = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 7.3mA (typ), DVDD= 1.6mA (typ), TVDD= 0.3mA (typ).

Note 22. When EXT Slave Mode (PMPLL=M/S bits ="0"), PMADL=PMADR=PMDAC=PMHPL=PMHPR= PMVCM=PMBP=PMMP bits = "1", and PMPFIL = LPMIC = LPDA bits = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 6.5mA (typ), DVDD= 1.6mA (typ), TVDD= 0.1mA (typ).

Note 23. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMSL=PMVCM= PMPLL=PMBP=PMMP=M/S bits = "1", and LPMIC = LPDA bits = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 6.5mA (typ), DVDD= 1.4mA (typ), TVDD= 0.3mA (typ).

Note 24. When EXT Slave Mode (PMPLL=M/S bits ="0"), PMADL=PMADR=PMDAC=PMSL=PMVCM= PMBP=PMMP bits = "1", and PMPFIL = LPMIC = LPDA bits = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 5.7mA (typ), DVDD= 1.4mA (typ), TVDD= 0.1mA (typ).

Note 25. All digital input pins are fixed to TVDD or VSS2.

Note 26. When AVDD, DVDD, and TVDD are powered OFF.

■ Power Consumption on Each Operation Mode

Conditions: Ta=25°C; AVDD= SVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=VSS3= 0V; fs=44.1kHz,
LPF, HPF, Stereo Separation, 5-band Equalizer, ALC, DRC=OFF (PMPFIL = PMDRC bits = "0"),
External Slave Mode, BICK=64fs; LIN1/RIN1 input = No input; SDTI input = No input;
Headphone & Speaker & Line output = No load.

Mode	Power Management Bit							AVDD [mA]	DVDD [mA]	TVDD [mA]	SVDD [mA]	Total Power [mW]
	PMVCM	PMSL	PMDAC	PMADL	PMADR	PMHPL	PMHPR					
All Power-down	0	0	0	0	0	0	0	0	0	0	0	0
LIN1/RIN1 → ADC (Note 27)	1	0	0	1	1	0	0	2.70	0.76	0.03	0.01	10.4
LIN1(Mono)→ADC (Note 27)	1	0	0	1	0	0	0	1.54	0.63	0.03	0.01	6.3
DAC → HP (Note 28)	1	0	1	0	0	1	1	1.49	0.69	0.01	0.01	6.2
DAC → SPK (LOSEL bit = "0")	1	1	1	0	0	0	0	1.44	0.67	0.01	0.76	8.5
LIN1/RIN1 → ADC (Note 27) & DAC → HP (Note 28)	1	0	1	1	1	1	1	4.07	1.60	0.03	0.01	16.4
LIN1/RIN1 → ADC (Note 27) & DAC → SPK (LOSEL bit = "0")	1	1	1	1	1	0	0	4.03	1.54	0.03	0.76	18.6

Note 27. Low-power consumption mode (LPMIC bit = "1").
Note 28. Low-power consumption mode (LPDA bit = "1").

Table 1. Power Consumption for Each Operation Mode (typ)

ADC SHARP ROLL-OFF FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V; SDAD bit = "0")

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 29)	+0.08dB ~ –0.23dB	PB	0	-	18.8	kHz
	–0.74dB		-	19.4	-	kHz
	–1.41dB		-	19.9	-	kHz
	–8.0dB		-	22.1	-	kHz
Stopband (Note 29)		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	62	-	-	dB
Group Delay (Note 30)		GD	-	10.7	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	3.4	-	Hz
(Note 29)	–0.5dB		-	10	-	Hz
	–0.1dB		-	22	-	Hz

ADC SHARP ROLL-OFF FILTER CHARACTERISTICS (fs=96kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V; SDAD bit = "0")

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 29)	+0.08dB ~ –0.23dB	PB	0	-	40.9	kHz
	–0.74dB		-	42.2	-	kHz
	–1.41dB		-	43.3	-	kHz
	–8.0dB		-	48.0	-	kHz
Stopband (Note 29)		SB	56.8	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	62	-	-	dB
Group Delay (Note 30)		GD	-	10.7	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	7.4	-	Hz
(Note 29)	–0.5dB		-	21.8	-	Hz
	–0.1dB		-	47.9	-	Hz

Note 29. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 30. A calculating delay time which induced by digital filtering. This time is from the input of an analog signal to the setting of 32-bit data of both channels to the ADC output register. For the signal through the programmable filters (First HPF + 4-band Equalizer + ALC + Equalizer), the group delay is increased 4/fs from the value above if there is no phase change by the IIR filter.

ADC SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V; SDAD bit = "1")

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 33)	+0.08dB ~ –0.23dB	PB	0	-	18.8	kHz
	–0.74dB		-	19.4	-	kHz
	–1.41dB		-	19.9	-	kHz
	–8.0dB		-	22.1	-	kHz
Stopband (Note 33)		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	61	-	-	dB
Group Delay (Note 34)		GD	-	4.3	-	1/fs
Group Delay Distortion		ΔGD	-	-	±1.8	1/fs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	3.4	-	Hz
(Note 31)	–0.5dB		-	10	-	Hz
	–0.1dB		-	22	-	Hz

ADC SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS (fs=96kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V; SDAD bit = "1")

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 33)	+0.08dB ~ –0.23dB	PB	0	-	40.9	kHz
	–0.74dB		-	42.2	-	kHz
	–1.41dB		-	43.3	-	kHz
	–8.0dB		-	48.0	-	kHz
Stopband (Note 31)		SB	56.8	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	61	-	-	dB
Group Delay (Note 32)		GD	-	4.3	-	1/fs
Group Delay Distortion		ΔGD	-	-	±1.3	1/fs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	7.4	-	Hz
(Note 31)	–0.5dB		-	21.8	-	Hz
	–0.1dB		-	47.9	-	Hz

Note 31. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 32. A calculating delay time which induced by digital filtering. This time is from the input of an analog signal to the setting of 32-bit data of both channels to the ADC output register. For the signal through the programmable filters (First HPF + 4-band Equalizer + ALC + Equalizer), the group delay is increased 4/fs from the value above if there is no phase change by the IIR filter.

DAC FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF):						
Passband (Note 33)	±0.05dB −6.0dB	PB	0 -	- 22.05	20.0 -	kHz kHz
Stopband (Note 33)		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 34)		GD	-	22	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz (Note 33)		FR	-	±1.0	-	dB

DAC FILTER CHARACTERISTICS (fs=96kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF):						
Passband (Note 33)	±0.05dB −6.0dB	PB	0 -	- 48.0	43.5 -	kHz kHz
Stopband (Note 33)		SB	52.5	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 34)		GD	-	22	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 40.0kHz (Note 33)		FR	-	±1.0	-	dB

Note 33. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 34. A calculating delay time which induced by digital filtering. This time is from setting the 32-bit data of both channels to input register to the output of analog signal. For the signal through the programmable filters (First HPF + 4-band Equalizer + ALC + Equalizer), the group delay is increased 7/fs from the value above if there is no phase change by the IIR filter.

DC CHARACTERISTICS

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	min	typ	max	Unit
Audio Interface & Serial µP Interface (SDA, SCL, PDN, BICK, LRCK, SDTI, MCKI pins)						
High-Level Input Voltage	(TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
	(TVDD < 2.2V)		80%TVDD	-	-	V
Low-Level Input Voltage	(TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
	(TVDD < 2.2V)		-	-	20%TVDD	V
Audio Interface & Serial µP Interface (SDA, BICK, LRCK, SDTO, OVF pins Output)						
High-Level Output Voltage	(Iout = −80µA)	VOH	TVDD−0.2	-	-	V
Low-Level Output Voltage						
	(Except SDA pin : Iout = 80µA)	VOL1	-	-	0.2	V
	(SDA pin, 2.0V ≤ TVDD ≤ 3.5V: Iout = 3mA)	VOL2	-	-	0.4	V
	(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Input Leakage Current		Iin	-	-	±10	µA
Digital Microphone Interface (DMDAT pin Input ; DMIC bit = "1")						
High-Level Input Voltage		VIH3	65%AVDD	-	-	V
Low-Level Input Voltage		VIL3	-	-	35%AVDD	V
Sink Current	(Vin = AVDD)	Isink	-	-	150	µA
Source Current	(Vin = 0V)	Isource	-20	-	-	µA
Digital Microphone Interface (DMCLK pin Output ; DMIC bit = "1")						
High-Level Output Voltage	(Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage	(Iout= 80µA)	VOL3	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	µA

SWITCHING CHARACTERISTICS

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V; C_L=20pF)

Parameter		Symbol	min	typ	max	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing						
Frequency		fs	8	-	96	kHz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency		fs	8	-	96	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period	PLL2-0 bits = "000"	tBCK	-	1/(32fs)	-	ns
	PLL2-0 bits = "001"	tBCK	-	1/(64fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter			Symbol	min	typ	max	Unit
External Slave Mode							
MCKI Input Timing							
	Frequency	256fs	fCLK	2.048	-	24.576	MHz
		384fs	fCLK	3.072	-	18.432	MHz
		512fs	fCLK	4.096	-	24.576	MHz
		1024fs	fCLK	8.192	-	12.288	MHz
	Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
	Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing							
	Frequency	256fs	fs	8	-	96	kHz
		384fs	fs	8	-	48	kHz
		512fs	fs	8	-	48	kHz
		1024fs	fs	8	-	12	kHz
	Duty		Duty	45	-	55	%
BICK Input Timing							
	Period		tBCK	156.25	-	-	ns
	Pulse Width Low		tBCKL	65	-	-	ns
	Pulse Width High		tBCKH	65	-	-	ns
External Master Mode							
MCKI Input Timing							
	Frequency	256fs	fCLK	2.048	-	24.576	MHz
		384fs	fCLK	3.072	-	18.432	MHz
		512fs	fCLK	4.096	-	24.576	MHz
		1024fs	fCLK	8.192	-	12.288	MHz
	Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
	Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing							
	Frequency		fs	8	-	96	kHz
	Duty Cycle		Duty	-	50	-	%
BICK Output Timing							
	Period	BCKO bit = “0”	tBCK	-	1/(32fs)	-	ns
		BCKO bit = “1”	tBCK	-	1/(64fs)	-	ns
	Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Units
Audio Interface Timing					
Master Mode					
BICK "↓" to LRCK Edge (Note 35)	tMBLR	–20	-	20	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	–35	-	35	ns
BICK "↓" to SDTO	tBSD	–35	-	35	ns
SDTI Hold Time	tSDH	25	-	-	ns
SDTI Setup Time	tSDS	20	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 35)	tLRB	25	-	-	ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	25	-	-	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	-	-	45	ns
BICK "↓" to SDTO	tBSD	-	-	45	ns
SDTI Hold Time	tSDH	25	-	-	ns
SDTI Setup Time	tSDS	20	-	-	ns
Control Interface Timing (I²C Bus Mode): (Note 36)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 37)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 35. BICK rising edge must not occur at the same time as LRCK edge.
Note 36. I²C-bus is a trademark of NXP B.V.
Note 37. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Parameter		Symbol	min	typ	max	Unit
Digital Audio Interface Timing; fs = 8kHz ~ 48kHz, C_L=100pF						
DMCLK Output Timing						
Period		tSCK	-	1/(64fs)	-	ns
Rising Time		tSRise	-	-	10	ns
Falling Time		tSFall	-	-	10	ns
Duty Cycle		dSCK	40	50	60	%
Audio Interface Timing						
DMDAT Setup Time		tSDS	50	-	-	ns
DMDAT Hold Time		tSDH	0	-	-	ns
Power-down & Reset Timing						
PDN Accept Pulse Width	(Note 38)	tAPD	1	-	-	µs
PDN Reject Pulse Width	(Note 38)	tRPD	-	-	50	ns
PMADL or PMADR "↑" to SDTO valid	(Note 39)					
ADRST1-0 bits = "00"		tPDV	-	2115	-	1/fs
ADRST1-0 bits = "01"		tPDV	-	4227	-	1/fs
ADRST1-0 bits = "10"		tPDV	-	267	-	1/fs
ADRST1-0 bits = "11"		tPDV	-	1059	-	1/fs
PMDML or PMDMR "↑" to SDTO valid	(Note 40)					
ADRST1-0 bits = "00"		tPDV	-	2115	-	1/fs
ADRST1-0 bits = "01"		tPDV	-	4227	-	1/fs
ADRST1-0 bits = "10"		tPDV	-	267	-	1/fs
ADRST1-0 bits = "11"		tPDV	-	1059	-	1/fs

Note 38. The AK4954A can be reset by bringing the PDN pin "L" upon power-up. The PDN pin must held "L" for more than 1µs for a certain reset. The AK4954A is not reset by the "L" pulse less than 50ns.
Note 39. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".
Note 40. This is the count of LRCK "↑" from the PMDML or PMDMR bit = "1".

■ Timing Diagram

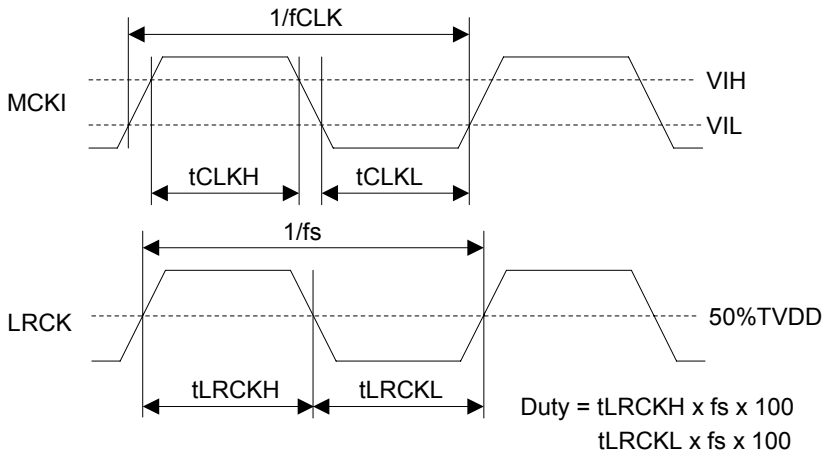


Figure 3. Clock Timing (PLL/EXT Master mode)

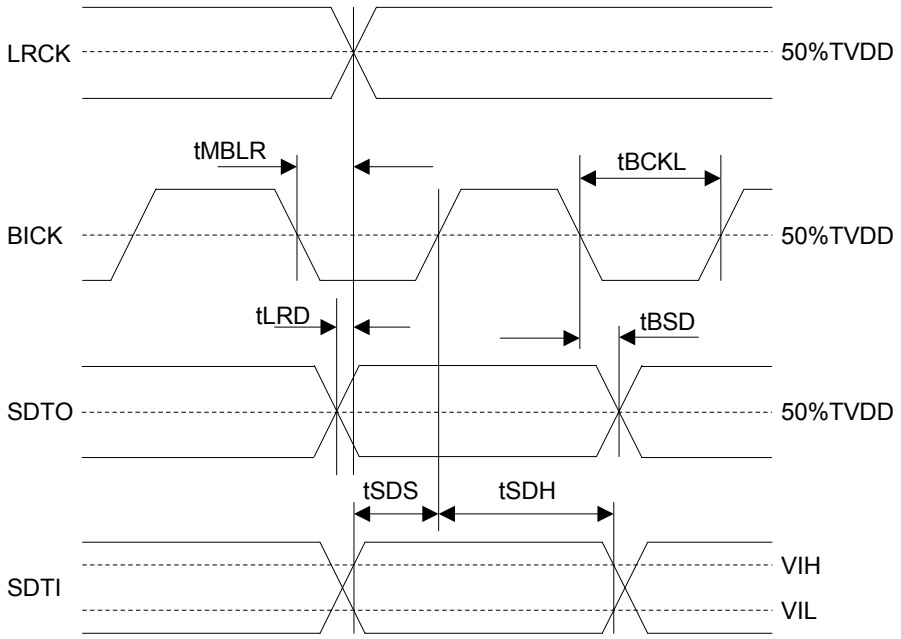


Figure 4. Audio Interface Timing (PLL/EXT Master mode)

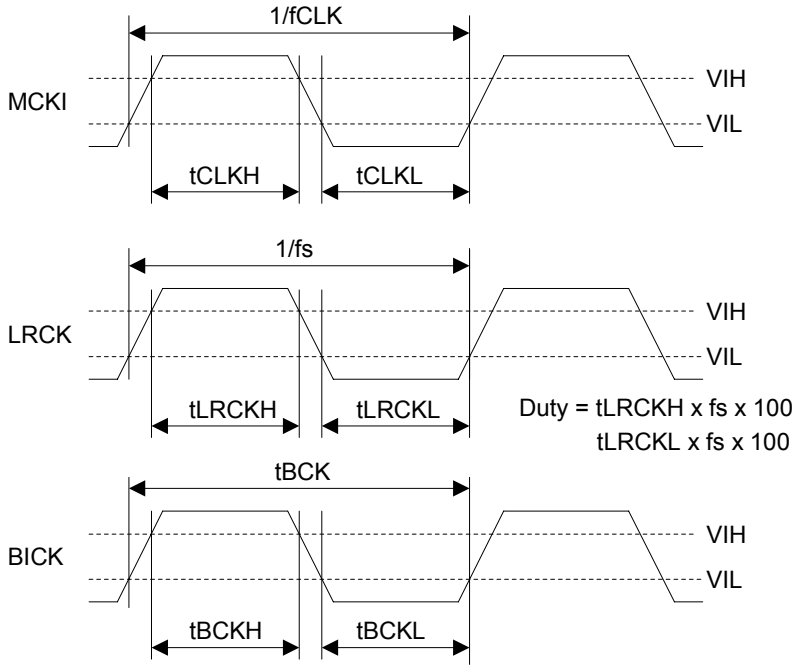


Figure 5. Clock Timing (EXT Slave mode)

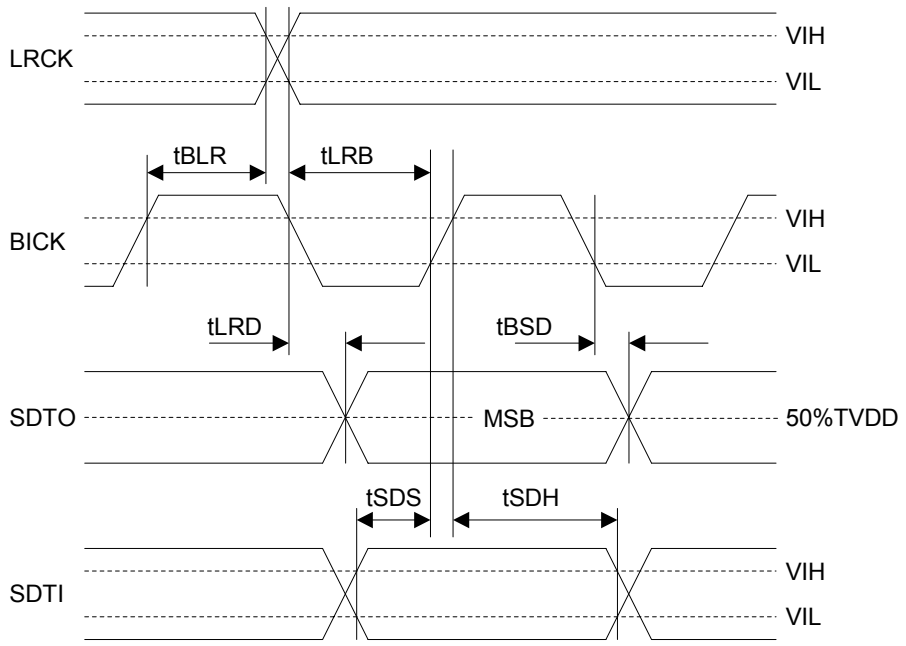


Figure 6. Audio Interface Timing (PLL/EXT Slave mode)

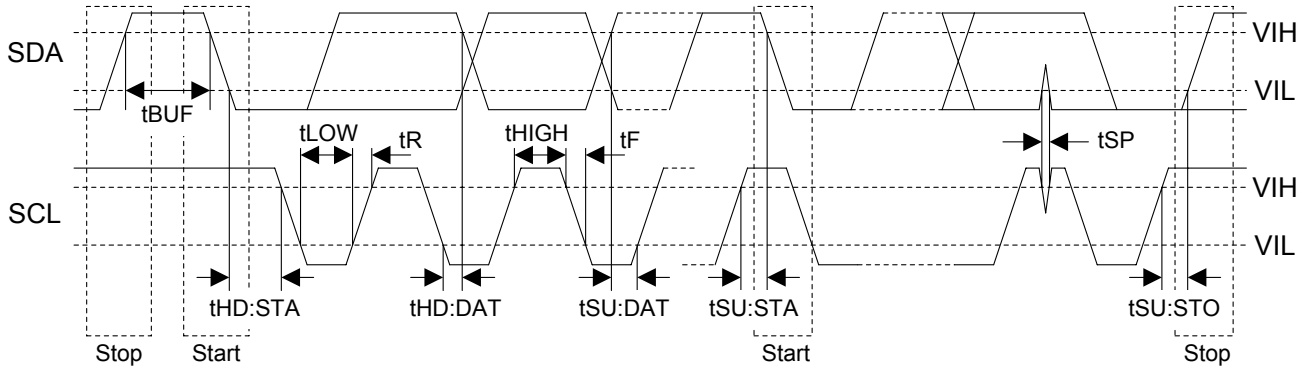
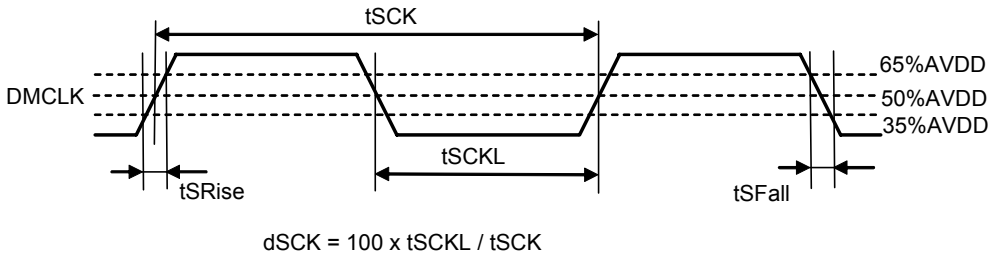


Figure 7. I^2C Bus Mode Timing



dSCK = 100 x tSCKL / tSCK

Figure 8. DMCLK Clock Timing

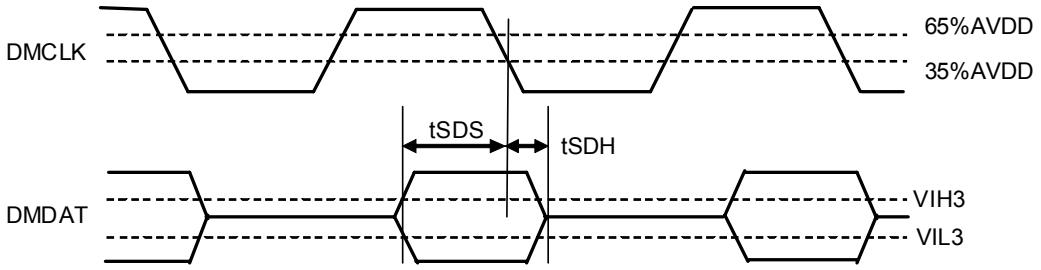


Figure 9. Audio Interface Timing (DCLKP bit = "1")

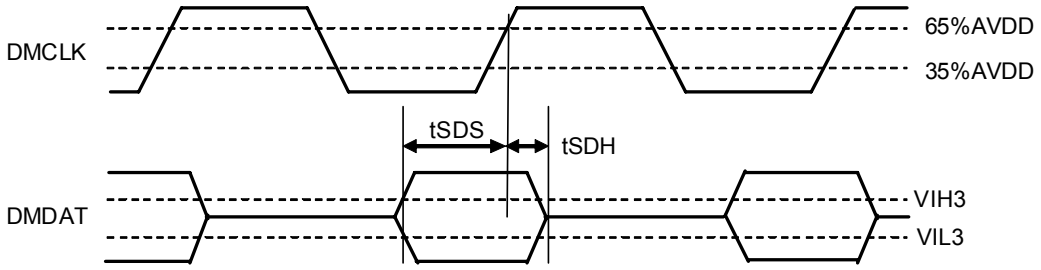


Figure 10. Audio Interface Timing (DCLKP bit = "0")

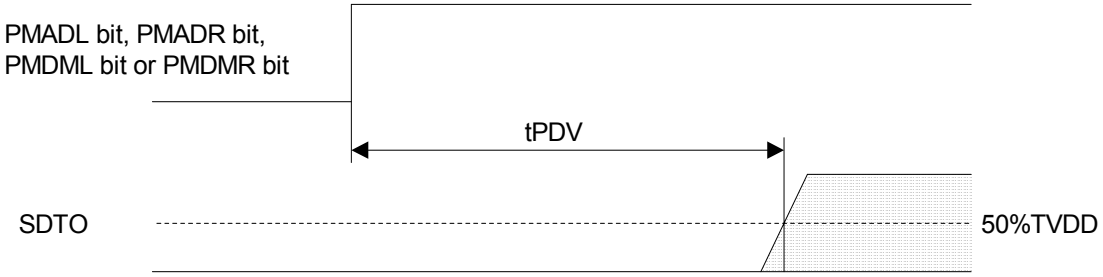


Figure 11. Power-down & Reset Timing 1

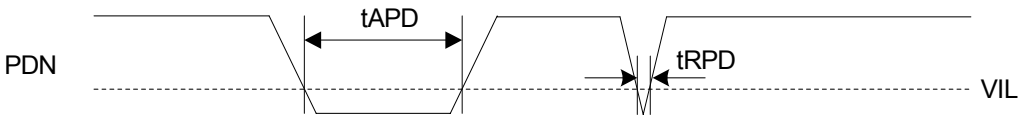


Figure 12. Power-down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following four clock modes to interface with external devices (Table 2, Table 3).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode	1	1	Table 5	Figure 13
PLL Slave Mode (PLL Reference Clock: MCKI pin)	1	0	Table 5	Figure 14
EXT Slave Mode	0	0	x	Figure 15
EXT Master Mode	0	1	x	Figure 16

Table 2. Clock Mode Setting (x: Don't care)

Mode	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	Input Frequency of Table 5 (Selected by PLL2-0 bits)	Output (Selected by BCKO bit)	Output (1fs)
PLL Slave Mode (PLL Reference Clock: BICK pin)	GND	Input (Selected by PLL2-0 bits)	Input (1fs)
EXT Slave Mode	Input Frequency of Table 5 (Selected by CM1-0 bits)	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	Input Frequency of Table 5 (Selected by CM1-0 bits)	Output (Selected by BCKO bit)	Output (1fs)

Table 3. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4954A is in power-down mode (PDN pin = "L") and when exits reset state, the AK4954A is in slave mode. After exiting reset state, the AK4954A goes to master mode by changing M/S bit = "1".

When the AK4954A is in master mode, the LRCK and BICK pins are a Hi-Z state until M/S bit becomes "1". The LRCK and BICK pins of the AK4954A must be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 4. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by the PLL2-0 and FS3-0 bits. The PLL lock times, when the AK4954A is supplied stable clocks or the sampling frequency is changed after PLL is powered-up (PMPLL bit = "0" → "1"), are shown in Table 5.

1) PLL Mode Setting

Mode	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)	
0	0	0	0	BICK pin	32fs	2ms	
1	0	0	1	BICK pin	64fs	2ms	
2	0	1	0	MCKI pin	11.2896MHz	10ms	(default)
3	0	1	1	MCKI pin	12.288MHz	10ms	
4	1	0	0	MCKI pin	12MHz	10ms	
5	1	0	1	MCKI pin	24MHz	10ms	
6	1	1	0	MCKI pin	13.5MHz	10ms	
7	1	1	1	MCKI pin	27MHz	10ms	

Table 5. PLL Mode Setting (*fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode

When the PLL reference clock input is the MCKI pin or the BICK pin, the sampling frequency is selected by FS3-0 bits as defined in Table 6.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (Note 41)	
0	0	0	0	0	8kHz mode	
1	0	0	0	1	11.025kHz mode	
2	0	0	1	0	12kHz mode	
4	0	1	0	0	16kHz mode	
5	0	1	0	1	22.05kHz mode	
6	0	1	1	0	24kHz mode	
8	1	0	0	0	32kHz mode	
9	1	0	0	1	44.1kHz mode	(default)
10	1	0	1	0	48kHz mode	
12	1	1	0	0	64kHz mode	
13	1	1	0	1	88.2kHz mode	
14	1	1	1	0	96kHz mode	
Others	Others				N/A	

Table 6. Setting of Sampling Frequency (N/A: Not Available)

Note 41. When the MCKI pin is the PLL reference clock input, the sampling frequency generated by PLL differs from the sampling frequency of mode name in some combinations of MCKI frequency(PLL2-0 bits) and sampling frequency (FS3-0 bits). Refer to Table 7 for the details of sampling frequency. In master mode, LRCK and BICK output frequency correspond to sampling frequencies shown in Table 7. When the BICK pin is the PLL reference clock input, the sampling frequency generated by PLL is the same sampling frequency of mode name.

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz] (Note 42)
12	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	64kHz mode	64.000000
	96kHz mode	96.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
	88.2kHz mode	88.199013
24	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	64kHz mode	64.000000
	96kHz mode	96.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
	88.2kHz mode	88.199013
13.5	8kHz mode	8.000300
	12kHz mode	12.000451
	16kHz mode	16.000601
	24kHz mode	24.000901
	32kHz mode	32.001202
	48kHz mode	48.001803
	64kHz mode	64.002404
	96kHz mode	96.003606
	11.025kHz mode	11.025218
	22.05kHz mode	22.050436
	44.1kHz mode	44.100871
	88.2kHz mode	88.201742
	Sampling frequency that differs from sampling frequency of mode name	

Note 42. These are rounded off to six decimal places.

Table 7. Sampling Frequency at PLL mode (Reference clock is MCKI)

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz] (Note 42)
27	8kHz mode	8.000300
	12kHz mode	12.000451
	16kHz mode	16.000601
	24kHz mode	24.000901
	32kHz mode	32.001202
	48kHz mode	48.001803
	64kHz mode	64.002404
	96kHz mode	96.003606
	11.025kHz mode	11.025218
	22.05kHz mode	22.050436
	44.1kHz mode	44.100871
	88.2kHz mode	88.201742
11.2896	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	64kHz mode	64.000000
	96kHz mode	96.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
	88.2kHz mode	88.200000
12.288	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	64kHz mode	64.000000
	96kHz mode	96.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
	88.2kHz mode	88.200000
Sampling frequency that differs from sampling frequency of mode name		

Note 42. These are rounded off to six decimal places.

Table 7. Sampling Frequency at PLL mode (Reference clock is MCKI) (2)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, LRCK and BICK pins go to "L" until the PLL goes to lock state after PMPLL bit = "0" → "1" (Table 8).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

PLL State	BICK pin	LRCK pin
After PMPLL bit "0" → "1"	"L" Output	"L" Output
PLL Unlock (except the case above)	Invalid	Invalid
PLL Lock	Table 9	1fs Output

Table 8. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12.288MHz, 13.5MHz, 24MHz or 27MHz) is input to the MCKI pin, the internal PLL circuit generates BICK and LRCK clocks. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 9).

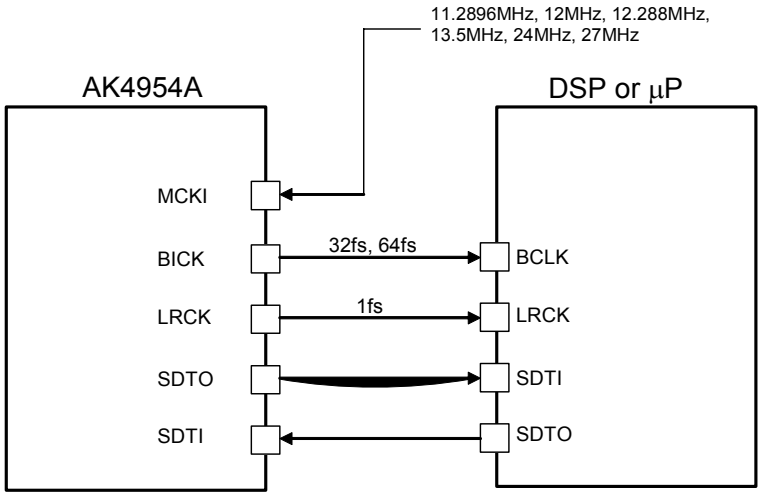


Figure 13. PLL Master Mode

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 9. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to the BICK pin. The required clock for the AK4954A is generated by an internal PLL circuit. Input frequency is selected by PLL2-0 bits (Table 5).

The BICK and LRCK inputs must be synchronized. Sampling frequency can be selected by FS3-0 bits. (Table 6)

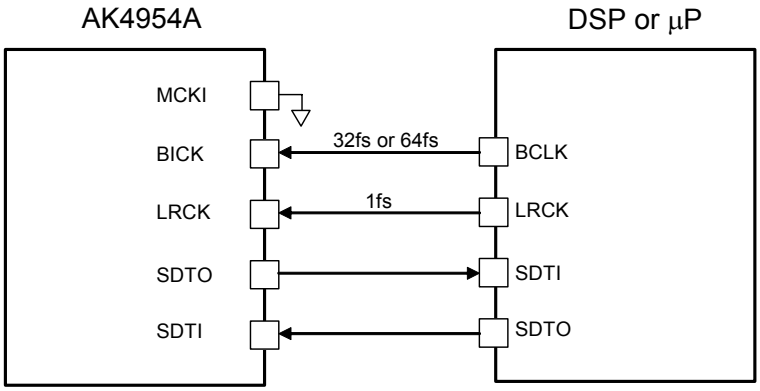


Figure 14. PLL Slave Mode (PLL Reference Clock: BICK pin)

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4954A becomes EXT mode. Master clock can be input to the internal ADC and DAC directly from the MCKI pin without internal PLL circuit operation. This mode is compatible with I/F of a normal audio CODEC. The external clocks required to operate this mode are MCKI (256fs, 384fs, 512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) must be synchronized with LRCK. The phase between these clocks is not important. The input frequency of MCKI is selected by CM1-0 bits (Table 10) and the sampling frequency is selected by FS3-0 bits (Table 11).

Mode	CM1 bit	CM0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	0	0	256fs	8kHz ≤ fs ≤ 96kHz	(default)
1	0	1	384fs	8kHz < fs ≤ 48kHz	
2	1	0	512fs	8kHz < fs ≤ 48kHz	
3	1	1	1024fs	8kHz ≤ fs ≤ 24kHz	

Table 10. MCKI Frequency Select in EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	
1	0	0	0	1	11.025kHz	
2	0	0	1	0	12kHz	
4	0	1	0	0	16kHz	
5	0	1	0	1	22.05kHz	
6	0	1	1	0	24kHz	
8	1	0	0	0	32kHz	
9	1	0	0	1	44.1kHz	(default)
10	1	0	1	0	48kHz	
12	1	1	0	0	64kHz	
13	1	1	0	1	88.2kHz	
14	1	1	1	0	96kHz	
Others	Others				N/A	

Table 11. Sampling Frequency Setting (N/A: Not Available)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through HPL/HPR pins is shown in Table 12.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	87 dB
384fs	87 dB
512fs	97 dB
1024fs	100 dB

Table 12. Relationship between MCKI and S/N of HPL/HPR pins

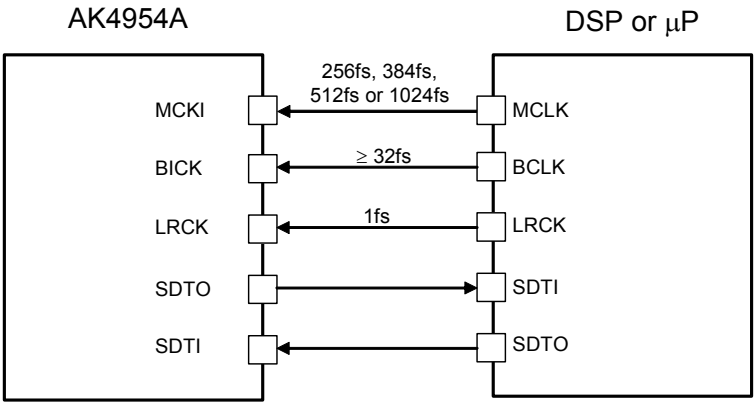


Figure 15. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The AK4954A becomes EXT Master Mode by setting PMPLL bit = "0" and M/S bit = "1". Master clock can be input to the internal ADC and DAC directly from the MCKI pin without the internal PLL circuit operation. The external clock required to operate the AK4953A is MCKI (256fs, 384fs, 512fs or 1024fs). The input frequency of MCKI is selected by CM1-0 bits (Table 13). The sampling frequency is selected by FS3-0 bits (Table 14).

Mode	CM1 bit	CM0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	0	0	256fs	8kHz ≤ fs ≤ 96kHz	(default)
1	0	1	384fs	8kHz < fs ≤ 48kHz	
2	1	0	512fs	8kHz < fs ≤ 48kHz	
3	1	1	1024fs	8kHz ≤ fs ≤ 24kHz	

Table 13. MCKI Frequency in EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	
1	0	0	0	1	11.025kHz	
2	0	0	1	0	12kHz	
4	0	1	0	0	16kHz	
5	0	1	0	1	22.05kHz	
6	0	1	1	0	24kHz	
8	1	0	0	0	32kHz	
9	1	0	0	1	44.1kHz	(default)
10	1	0	1	0	48kHz	
12	1	1	0	0	64kHz	
13	1	1	0	1	88.2kHz	
14	1	1	1	0	96kHz	
Others	Others				N/A	

Table 14. Sampling Frequency Setting (N/A: Not Available)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through HPL/HPR pins is shown in Table 15.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	87 dB
384fs	87 dB
512fs	97 dB
1024fs	100 dB

Table 15. Relationship between MCKI and S/N of HPL/HPR pins

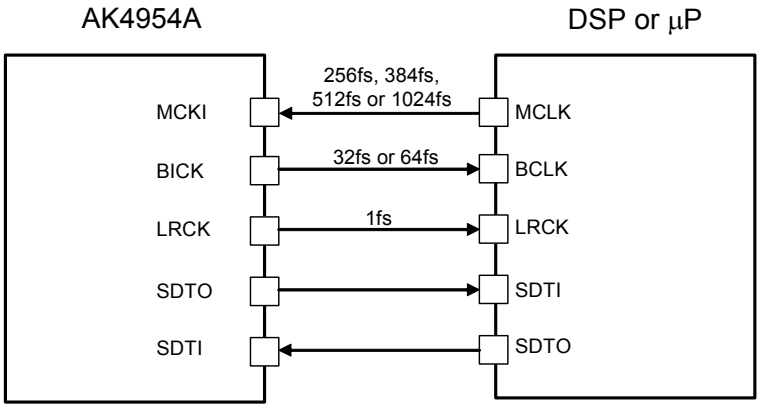


Figure 16. EXT Master Mode

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 16. BICK Output Frequency in Master Mode

■ System Reset

Upon power-up, the AK4954A must be reset by bringing the PDN pin = “L”. This reset is released when a dummy command is input after the PDN pin = “H”. This ensures that all internal registers reset to their initial value. This reset is released when the dummy command (Actually, the rising edge of 16th SCL) is input after PDN pin = “H”. Dummy command is executed by writing all “0” to the register address 00H. It is recommended to set the PDN pin = “L” before power up the AK4954A.

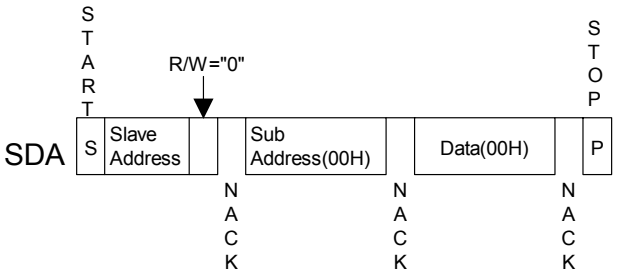


Figure 17. Dummy Command in I²C-bus Mode

The ADC enters an initialization cycle when the PMADL or PMADR bit is changed from “0” to “1”. The initialization cycle time is set by ADRST1-0 bits (Table 17). During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's complement, “0”. The ADC output reflects the analog input signal after the initialization cycle is complete. When using a digital microphone, the initialization cycle is the same as ADC’s.

Note 43. The initial data of ADC has offset data that depends on the condition of the microphone and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer by setting ADRST1-0 bits or do not use the initial data of ADC.

ADRST1 bit	ADRST0 bit	Initialization Cycle					
		Cycle	fs = 8kHz	fs = 16kHz	fs = 44.1kHz	fs = 96kHz	
0	0	2115/fs	264.4ms	132.2ms	48.0ms	22.0ms	(default)
0	1	4227/fs	528.4ms	264.2ms	95.9ms	44.0ms	
1	0	267/fs	33.4ms	16.7ms	6.1ms	2.8ms	
1	1	1059/fs	132.4ms	66.2ms	24.0ms	11.0ms	

Table 17. ADC Initialization Cycle

■ Audio Interface Format

Six types of data formats are available and selected by setting the DIF2-0 bits (Table 18). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK4954A in master mode, but must be input to the AK4954A in slave mode. The SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑") of BICK.

Mode	DIF2 bit	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	0	24-bit MSB justified	24-bit LSB justified	≥ 48fs	Figure 18	
1	0	0	1	24-bit MSB justified	16-bit LSB justified	≥ 32fs	Figure 19	
2	0	1	0	24-bit MSB justified	24-bit MSB justified	≥ 48fs	Figure 20	(default)
3	0	1	1	24-bit/16bit I^{2}S Compatible		=32fs or ≥ 48fs	Figure 21	
4	1	1	0	32-bit MSB justified	32-bit MSB justified	≥ 64fs	Figure 22	
5	1	1	1	32-bit I^{2}S Compatible		≥ 64fs	Figure 23	
Others	Others			N/A				

Table 18. Audio Interface Format (N/A: Not available)

If 32, 24 or 16-bit data, the output of ADC, is converted to an 8-bit data by removing LSB 24, 16 or 8-bit, "–1" data is converted to "–1" of 8-bit data. And when the DAC playbacks this 8-bit data, "–1" of 8-bit data will be converted to "-16777216", "–65536" or "-256"of 32, 24 or 16-bit data which is a large offset. This offset can be removed by adding the offset of "8388608", "32768" and "128" to 32, 24 and 16-bit data, respectively before converting to 8-bit data.

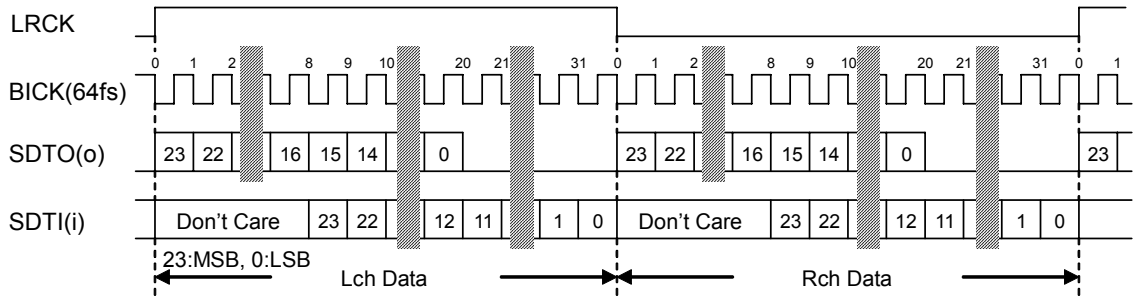


Figure 18. Mode 0 Timing

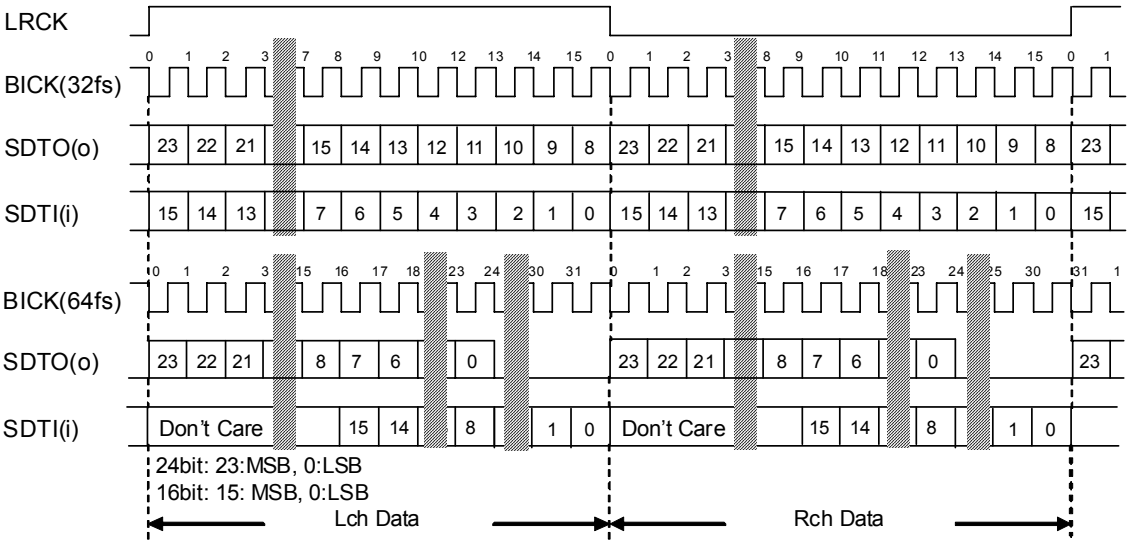


Figure 19. Mode 1 Timing

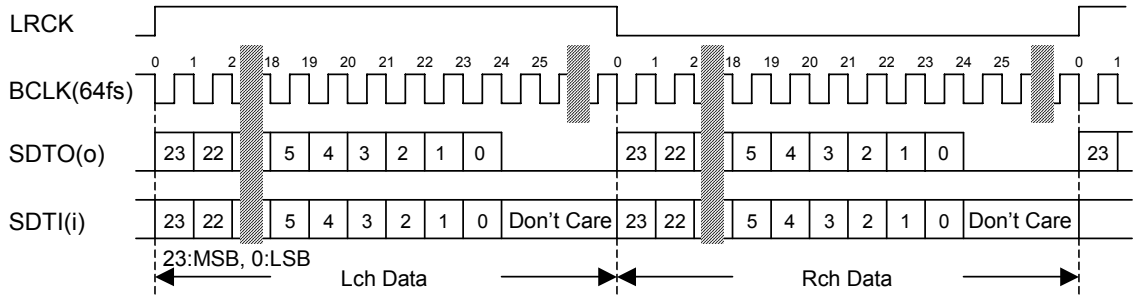


Figure 20. Mode 2 Timing

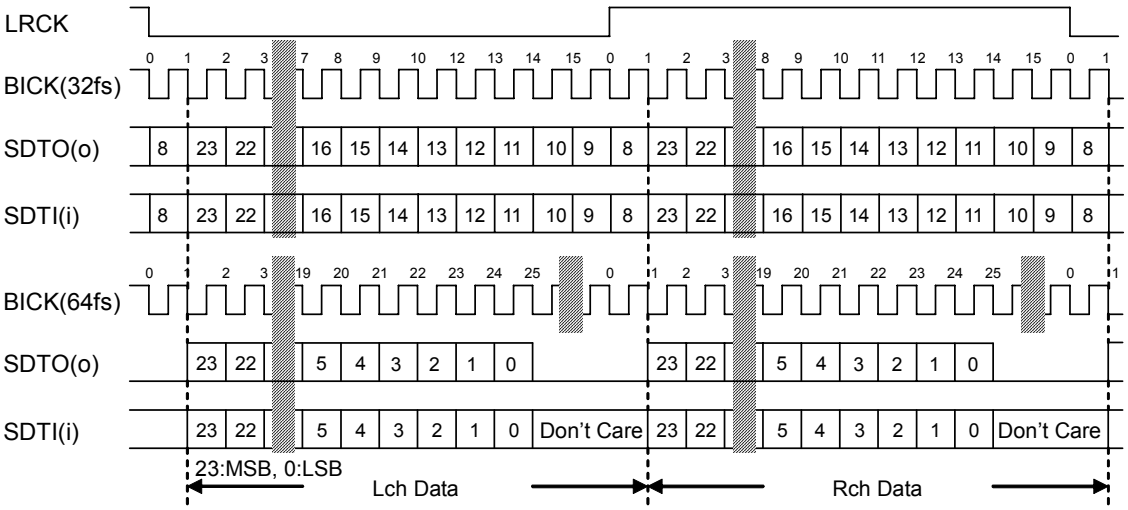


Figure 21. Mode 3 Timing

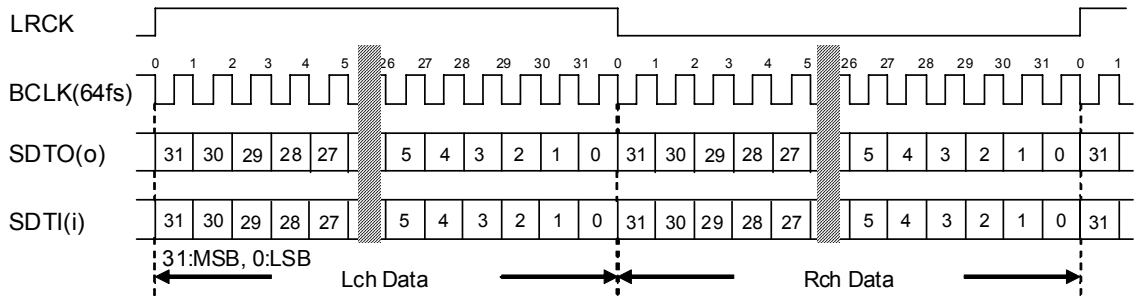


Figure 22. Mode 4 Timing

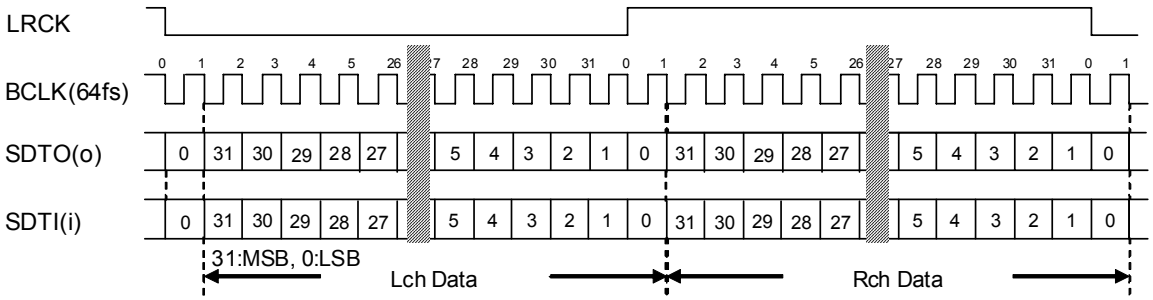


Figure 23. Mode 5 Timing

■ Mono/Stereo Mode

PMADL, PMADR, PMDML and PMDMR bits set mono/stereo ADC operation. When changing ADC operation and analog/digital microphone, PMADL, PMADR, PMDML and PMDMR bits must be set "0" at first. When DMIC bit = "1", PMADL and PMADR bit settings are ignored. When DMIC bit = "0", PMDML and PMDMR bit settings are ignored.

PMADL bit	PMADR bit	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 19. Mono/Stereo ADC operation (Analog Microphone)

PMDML bit	PMDMR bit	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 20. Mono/Stereo ADC operation (Digital Microphone)

■ Microphone/LINE Input Selector

The AK4954A has an input selector. INL1-0 and INR1-0 bits select LIN1/LIN2/LIN3 and RIN1/RIN2/RIN3, respectively. When DMIC bit = "1", digital microphone input is selected regardless of INL and INR bits.

DMIC bit	INL1 bit	INL0 bit	INR1 bit	INR0 bit	Lch	Rch	
0	0	0	0	0	LIN1	RIN1	(default)
	0	0	0	1	LIN1	RIN2	
	0	0	1	0	LIN1	RIN3	
	0	1	0	0	LIN2	RIN1	
	0	1	0	1	LIN2	RIN2	
	0	1	1	0	LIN2	RIN3	
	1	0	0	0	LIN3	RIN1	
	1	0	0	1	LIN3	RIN2	
	1	0	1	0	LIN3	RIN3	
	Others				N/A	N/A	
1	x	x	x	x	Digital Microphone		

Table 21. Microphone/Line In Path Select (x: Don't care, N/A: Not available)

■ Microphone Gain Amplifier

The AK4954A has a gain amplifier for microphone input. The gain of microphone amplifier is selected by the MGAIN2-0 bits (Table 22). PMADL and PMADR bits must be "0" when changing the MGAIN2-0 bits setting. The typical input resistance is 100kΩ.

MGAIN2 bit	MGAIN1 bit	MGAIN0 bit	Input Gain	
1	x	x	0dB	
0	0	0	+6dB	
0	0	1	+13dB	
0	1	0	+20dB	(default)
0	1	1	+26dB	

Table 22. Input Gain (x: Don't care)

<Low-power Consumption Mode>

LPMIC bit controls operation mode of the microphone amplifier. Low-power consumption mode is valid when the fs=8kHz ~ 48kHz.

LPMIC bit	Mode	Power Consumption (MIC+ADC → SDTO)	S/N (A-weighted)	S/(N+D) (-1dBFS)	
0	Normal	13.6mW	97dB	88dB	(default)
1	Low-power Consumption	10.4mW	96dB	80dB	

Table 23. Microphone Amplifier Operation Mode (MGAIN2-0 bits = "010": +20dB)

■ Microphone Power

When PMMP bit = "1", the MPWR1 or MPWR2 pin supplies power for the microphones. This output voltage is typically 2.64V (0.8 x AVDD) and the load resistance is minimum 1kΩ. In case of using two sets of stereo microphones, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWR1 and MPWR2 pins (Figure 24).

PMMP bit	MPSEL bit	Output	
0	x	Hi-Z	(default)
1	0	MPWR1 pin	
	1	MPWR2 pin	

Table 24. Microphone Power (x: Don't care)

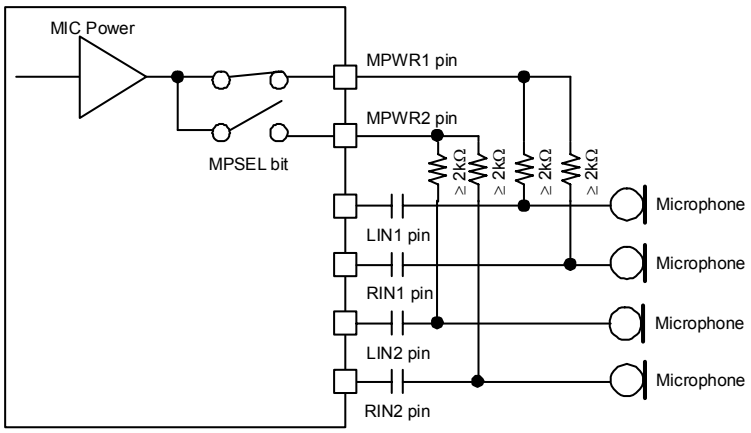


Figure 24. Microphone Block Circuit

■ Digital Microphone

1. Connection to Digital Microphones

The AK4954A can be connected to a digital microphone by setting DMIC bit = "1", and it supports sampling frequency up to 48kHz. When DMIC bit is set to "1", the LIN1 and RIN1 pins become DMDAT (digital microphone data input) and DMCLK (digital microphone clock supply) pins respectively. The same voltage as AVDD must be provided to the digital microphone. The Figure 25 and Figure 26 show mono/stereo connection examples. The DMCLK signal is output from the AK4954A, and the digital microphone outputs 1-bit data, which generated by ΔΣModulator using, from DMDAT. PMDML/R bits control power up/down of the digital block (Decimation Filter and Digital Filter). PMADL/PMADR bits settings do not affect the digital microphone power management. The DCLKE bit controls ON/OFF of the output clock from the DMCLK pin. When the AK4954A is powered down (PDN pin= "L"), the DMCLK and DMDAT pins are floating state. Pull-down resistors must be connected to the DMCLK and DMDAT pins externally to avoid this floating state.

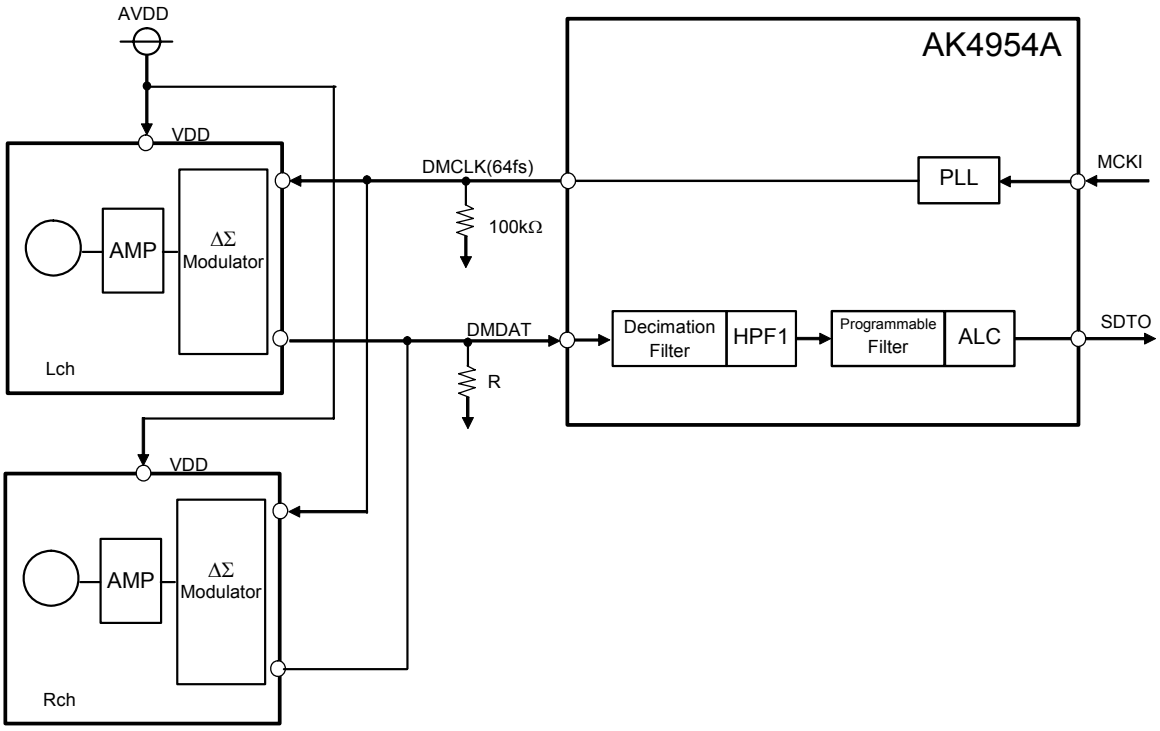


Figure 25. Connection Example of Stereo Digital Microphone

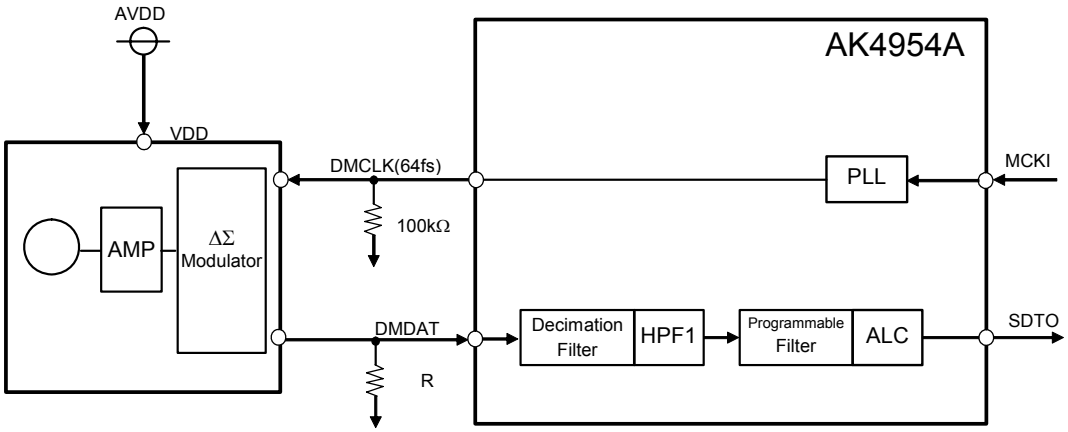


Figure 26. Connection Example of Mono Digital Microphone

2. Interface

The input data channel of the DMDAT pin is set by DCLKP bit. When DCLKP bit = "1, Lch data is input to the decimation filter if the DMCLK pin= "H", and Rch data is input if the DMCLK pin= "L". When DCLKP bit = "0", Rch data is input to the decimation filter if the DMCLK pin= "H", and Lch data is input if the DMCLK pin= "L". The DMCLK pin outputs "L" when DCLKE bit = "0", and only supports 64fs. In this case, necessary clocks must be supplied to the AK4954A for ADC operation. The output data through "the Decimation and Digital Filters" is 32-bit full scale when the 1bit data density is 0%~100%.

DCLKP bit	DMCLK pin= "H"	DMCLK pin= "L"	
0	Rch	Lch	(default)
1	Lch	Rch	

Table 25. Data In/Output Timing with Digital Microphone

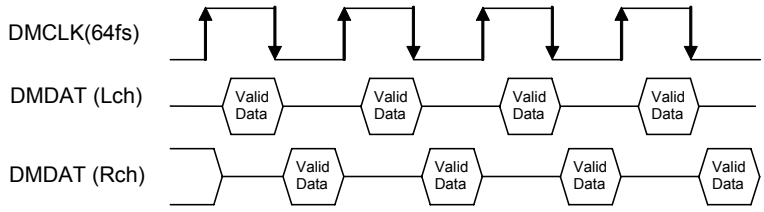


Figure 27. Data In/Output Timing with Digital Microphone (DCLKP bit = "1")

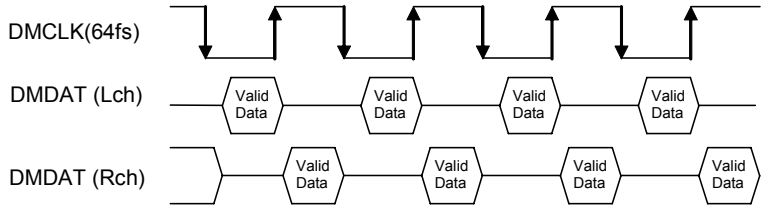
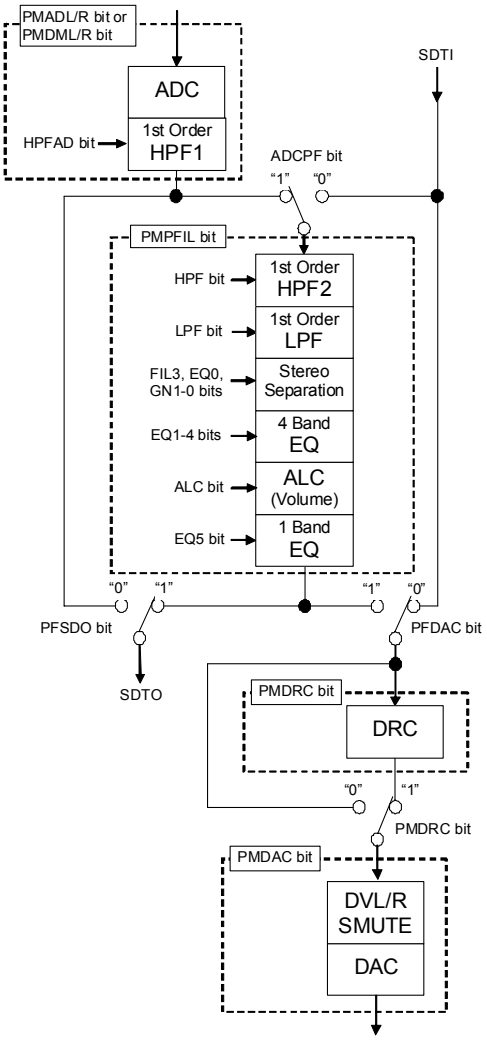


Figure 28. Data In/Output Timing with Digital Microphone (DCLKP bit = "0")

■ Digital Block

The digital block consists of the blocks shown in Figure 29. Recording path and playback path is selected by setting ADCPF bit, PFDAC bit and PFSDO bit. (Figure 30 ~ Figure 33, Table 26)



(1) ADC: Includes the Digital Filter (LPF) for ADC as shown in "FILTER CHRACTERISTICS".
(2) HPF1: Includes the Digital Filter (HPF) for ADC as shown in "FILTER CHRACTERISTICS".
(3) DAC: Includes the Digital Filter (LPF) for DAC as shown in "FILTER CHRACTERISTICS".
(4) HPF2: High Pass Filter. Applicable for use as Wind-Noise Reduction Filter. (See "Digital Programmable Filter Circuit")
(5) Stereo Separation: Stereo separation emphasis filter and gain compensation. (See "Digital Programmable Filter Circuit") Gain compensation consists of EQ0 and Gain control. It corrects frequency characteristics after stereo separation emphasis filter.
(6) LPF: Low Pass Filter (See "Digital Programmable Filter Circuit")
(7) 4 Band EQ: Applicable for use as Equalizer or Notch Filter. (See "Digital Programmable Filter Circuit")
(8) Volume: Input Digital Volume with ALC function. (See "Input Digital Volume" and "ALC Operation")
(9) 1 Band EQ: Applicable for use as Equalizer or Notch Filter. (See "Digital Programmable Filter Circuit")
(10) DRC: Dynamic range control circuit for playback path. (See "DRC Operation")
(11) DVL/R, SMUTE: Digital volume with soft mute function for playback path (See "Output Digital Volume2")

Figure 29. Digital Block Path Select

Mode	ADCPF bit	PFDAC bit	PFSDO bit	PMDRC bit	Figure
Recording Mode 1	1	0	1	0	Figure 30
Playback Mode 1	0	1	0	0	Figure 31
Recording Mode 2 (Programmable Filter Bypass Mode: PMPFIL bit = "0")	x	0	0	1	Figure 32
Loopback Mode	1	1	1	0	Figure 33

Table 26. Recording Playback Mode (x: Don't care)

LPF bit, HPF bit, EQ0 bit, EQ1 bit, EQ2 bit, EQ3 bit, EQ4 bit, EQ5 bit, and ALC bit must be "0" when changing those modes.

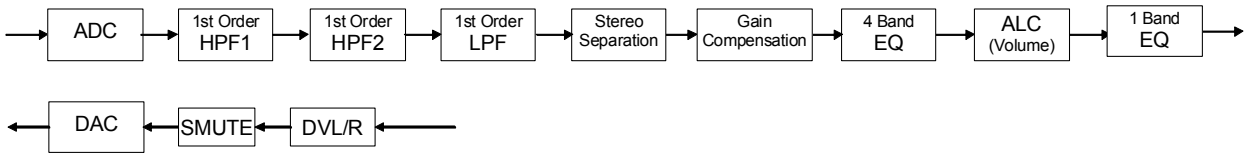


Figure 30. Path at Recording Mode 1 (default)

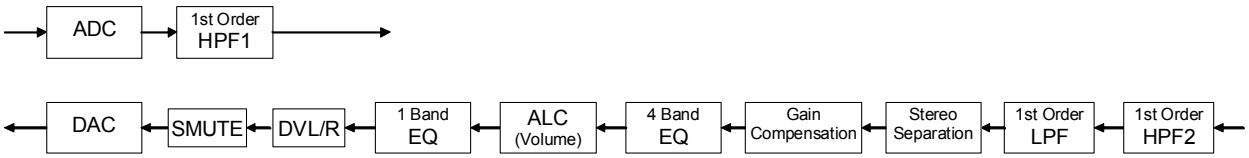


Figure 31. Path at Playback Mode 1

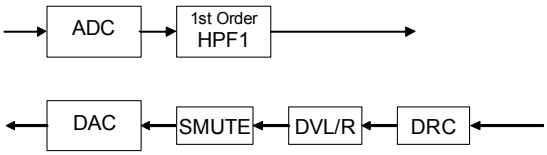


Figure 32. Path at Recording Mode 2 & Playback Mode 2

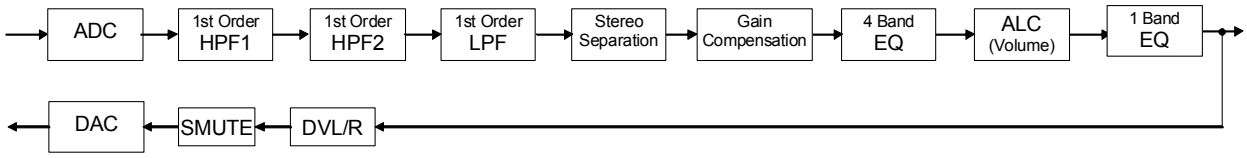


Figure 33. Path at Loopback Mode

■ Overflow Detection (OVF pin, OVFL bit = "1")

The AK4954A has an overflow detect function for the analog input. The overflow detect function is enabled when the PMPLL bit is set to "1" (PLL Slave Mode). The MCKI pin becomes the OVF pin by setting OVFL bit to "1" when PMPLL bit = "1" and PLL2-0 bits = "00x". (If PMPLL bit and PLL2-0 bits settings are different, the MCKI pin does not changed to the OVF pin by setting OVFL bit = "1") The OVF pin outputs "H" when the analog input of L or R channel overflows (more than -0.3dBFS). The output hold time is 128/fs (@OVTM1-0 bits = "10"). When the analog input is overflowed, the output signal of the OVF pin has the same group delay as ADC. The OVF pin outputs "L" during ADC initializing period after power up ADC (PMADL or PMADR bit = "0" → "1"), and then overflow detection is enabled.

OVTM1 bit	OVTM0 bit	Overflow Output Hold Time				
		Setting	fs=8kHz	fs=44.1kHz	fs=96kHz	
0	0	16/fs	2ms	0.4ms	0.2ms	
0	1	64/fs	8ms	1.5ms	0.7ms	
1	0	128/fs	16ms	2.9ms	1.3ms	(default)
1	1	256/fs	32ms	5.8ms	2.7ms	

Table 27. Overflow Output Hold Time Setting

■ Digital Filter

The AK4954A has two types of digital filters for ADC. Sharp roll-off filter or short delay sharp roll-off filter can be selected by setting SDAD bit.

SDAD bit	ADC	
0	Sharp Roll Off Filter	(default)
1	Short Delay Sharp Roll Off Filter	

Table 28. ADC Digital Filter Selection

■ Digital HPF1

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequencies of the HPF1 are set by HPFC1-0 bits (Table 29). It is proportional to the sampling frequency (fs) and default is 3.4Hz (@fs = 44.1kHz). HPFAD bit controls the ON/OFF of the HPF1 (HPF ON is recommended).

HPFC1 bit	HPFC0 bit	fc				
		fs=96kHz	fs=44.1kHz	fs=22.05kHz	fs=8kHz	
0	0	0.62Hz	1.7Hz	3.4Hz	7.5Hz	(default)
0	1	2.49Hz	6.9Hz	13.7Hz	29.8Hz	
1	0	19.9Hz	54.8Hz	109.7Hz	238.7Hz	
1	1	39.8Hz	109.7Hz	219.3Hz	477.5Hz	

Table 29. HPF1 Cut-off Frequency

■ Digital Programmable Filter Circuit

(1) High Pass Filter (HPF2)

Normally, this HPF is used for Wind-Noise Reduction. This is composed 1st order HPF. The coefficient of HPF is set by F1A13-0 bits and F1B13-0 bits. HPF bit controls ON/OFF of the HPF2. When the HPF2 is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when HPF bit = "0" or PMPFIL bit = "0". The HPF2 starts operation 4/fs(max) after when HPF bit=PMPFIL bit= "1" is set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 44)
HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.0001 (fc min = 4.41Hz at 44.1kHz)

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when LPF bit = "0" or PMPFIL bit = "0". The LPF starts operation 4/fs(max) after when LPF bit =PMPFIL bit= "1" is set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 44)
LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F2B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.05 (fc min = 2205Hz at 44.1kHz)

(3) Stereo Separation Emphasis Filter (FIL3)

The FIL3 is used to emphasize the stereo separation of stereo microphone recording data and playback data. F3A13-0 bits and F3B13-0 bits set the filter coefficients of the FIL3. When F3AS bit = "0", the FIL3 performs as a High Pass Filter (HPF), and it performs as a Low Pass Filter (LPF) when F3AS bit = "1". FIL3 bit controls ON/OFF of the FIL3. When the stereo separation emphasis filter is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when FIL3 bit or PMPFIL bit is "0". The FIL3 starts operation 4/fs(max) after when FIL3 bit =PMPFIL bit= "1" is set.

1) In case of setting FIL3 as HPF

fs: Sampling Frequency
fc: Cutoff Frequency
K: Gain [dB] (0dB ≥ K ≥ -10dB)

Register Setting (Note 44)
FIL3: F3AS bit = "0", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB=F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

2) In case of setting FIL3 as LPF

fs: Sampling Frequency
fc: Cutoff Frequency
K: Gain [dB] (0dB ≥ K ≥ −10dB)

Register Setting (Note 44)
FIL3: F3AS bit = "1", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB= F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

(4) Gain Compensation (EQ0)

Gain compensation is used to compensate the frequency response and the gain that is changed by the stereo separation emphasis filter. Gain compensation is composed of the Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). E0A15-0 bits, E0B13-0 bits and E0C15-0 bits set the coefficient of EQ0. GN1-0 bits set the gain (Table 35). EQ0 bit controls ON/OFF of EQ0. When EQ is OFF and the gain is 0dB, the audio data passes this block by 0dB gain. The coefficient should be set when EQ0 bit = "0" or PMPFIL bit = "0". The EQ0 starts operation 4/fs(max) after when EQ0 bit =PMPFIL bit= "1" is set.

fs: Sampling Frequency
fc_1: Polar Frequency
fc_2: Zero-point Frequency
K: Gain [dB] (Maximum setting is +12dB.)

Register Setting (Note 44)
E0A[15:0] bits =A, E0B[13:0] bits =B, E0C[15:0] bits =C
(MSB=E0A15, E0B13, E0C15; LSB=E0A0, E0B0, E0C0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

Transfer Function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

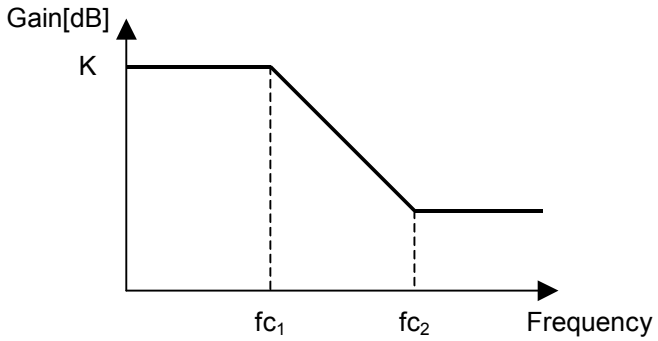


Figure 34. EQ0 Frequency Response

GN1 bit	GN0 bit	Gain	
0	0	0dB	(default)
0	1	+12dB	
1	x	+24dB	

Table 30. Gain Setting (x: Don't care)

(5) 4-band Equalizer & 1-band Equalizer after ALC

This block can be used as Equalizer or Notch Filter. A 4-band Equalizer (EQ1, EQ2, EQ3 and EQ4) is switched ON/OFF independently by EQ1, EQ2, EQ3 and EQ4 bits. The equalizer after ALC (EQ5) is controlled by EQ5 bit. When the Equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0, E1B15-0 and E1C15-0 bits set the coefficient of EQ1. E2A15-0, E2B15-0 and E2C15-0 bits set the coefficient of EQ2. E3A15-0, E3B15-0 and E3C15-0 bits set the coefficient of EQ3. E4A15-0, E4B15-0 and E4C15-0 bits set the coefficient of EQ4. E5A15-0, E5B15-0 and E5C15-0 bits set the coefficient of EQ5. The EQx (x=1~5) coefficient must be set when EQx bit = "0" or PMPFIL bit = "0". EQ1-5 start operation 4/fs(max) after when EQx (x=1~5) = PMPFIL bit = "1"is set.

fs: Sampling frequency
$fo_1 \sim fo_5$: Center frequency
$fb_1 \sim fb_5$: Band width where the gain is 3dB different from center frequency
$K_1 \sim K_5$: Gain ($-1 \le K_n \le 3$)

Register setting (Note 44)
EQ1: E1A[15:0] bits =A_1, E1B[15:0] bits =B_1, E1C[15:0] bits =C_1
EQ2: E2A[15:0] bits =A_2, E2B[15:0] bits =B_2, E2C[15:0] bits =C_2
EQ3: E3A[15:0] bits =A_3, E3B[15:0] bits =B_3, E3C[15:0] bits =C_3
EQ4: E4A[15:0] bits =A_4, E4B[15:0] bits =B_4, E4C[15:0] bits =C_4
EQ5: E5A[15:0] bits =A_5, E5B[15:0] bits =B_5, E5C[15:0] bits =C_5
(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15 ; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1+\tan(\pi fb_n/fs)}, \quad C_n = -\frac{1-\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer function

$$H(z) = \{1 + h_2(z) + h_3(z) + h_4(z) + h_5(z)\} \times \{1 + h_1(z)\}$$

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3, 4, 5)

The center frequency must be set as below.
$0.003 < fo_n / fs < 0.497$

When gain of K is set to "-1", this equalizer becomes a notch filter. When EQ1 ~EQ4 is used as a notch filter, central frequency of a real notch filter deviates from the above-mentioned calculation, if its central frequency of each band is near. The control soft that is attached to the evaluation board has functions that revises a gap of frequency and calculates the coefficient. When its central frequency of each band is near, the central frequency should be revised and confirm the frequency response.

Note 44. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X must be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sign bit.

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block when ALC bit is "1". When ADCPF bit is "1", ALC circuit operates at recording path. When ADCPF bit is "0", ALC circuit operates at playback path.

The ALC block consists of these blocks shown below. ALC limiter detection level and ALC recovery wait counter reset level are monitored at Level Detection 2 block after EQ block. The Level Detection 1 block also monitors clipping detection level (+0.53dBFS).

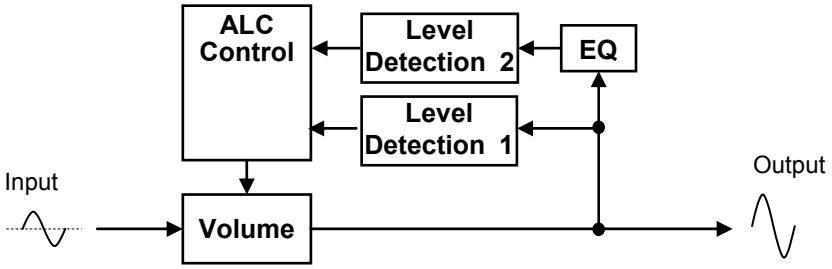


Figure 35. ALC Block

The polar (fc_1) and zero-point (fc_2) frequencies of EQ block are dependent on the sampling frequency. The coefficient is changed automatically according to the sampling frequency range setting. When ALC EQ block is OFF (ALCEQ bit = "1"), these level detection are off.

Sampling Frequency Range	Polar Frequency (fc1)	Zero-point Frequency (fc2)	
8kHz ≤ fs ≤ 12kHz	150Hz	100Hz	fs=11.025kHz
12kHz < fs ≤ 24kHz	150Hz	100Hz	fs=22.05kHz
24kHz < fs ≤ 48kHz	150Hz	100Hz	fs=44.1kHz
48kHz < fs ≤ 96kHz	150Hz	100Hz	fs=96kHz

Table 31. ALCEQ Frequency Setting

fs: Sampling Frequency
fc_1: Polar Frequency
fc_2: Zero-point Frequency

$$A = 10^{K/20} \times \frac{1 + 1/\tan(\pi fc_2/fs)}{1 + 1/\tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1/\tan(\pi fc_1/fs)}{1 + 1/\tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1/\tan(\pi fc_2/fs)}{1 + 1/\tan(\pi fc_1/fs)}$$

Transfer function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$

[ALCEQ: First order zero pole high pass filter]

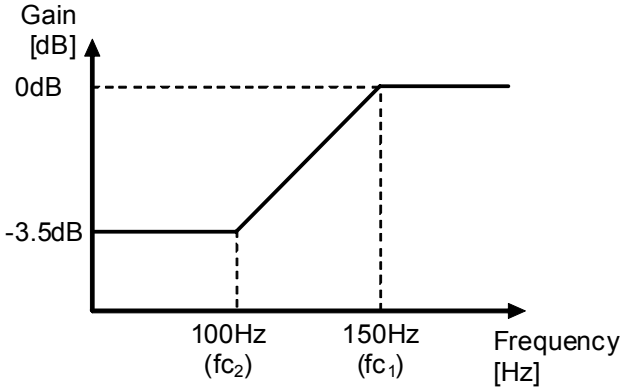


Figure 36. ALCEQ Frequency Response (fs = 44.1kHz)

1. ALC Limiter Operation

During ALC limiter operation, when either L or R channel output level exceeds the ALC limiter detection level (Table 32), the VOL value (same value for both L and R) is attenuated automatically according to the output level (Table 33). The volume is attenuated by the step amount shown in Table 33 at every sampling. (This attenuation is repeated for sixteen times once ALC limiter operation is executed.)

After completing the attenuate operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds ALC limiter detection level.

LMTH1 bit	LMTH0 bit	ALC Limiter Detection Level (LM-LEVEL)	ALC Recovery Waiting Counter Reset Level	
0	0	–2.5dBFS	–4.1dBFS	(default)
0	1	–4.1dBFS	–6.0dBFS	
1	0	–6.0dBFS	–8.5dBFS	
1	1	–8.5dBFS	–12dBFS	

Table 32. ALC Limiter Detection Level / Recovery Counter Reset Level

Output Level	ATT Step [dB]
+0.53dBFS ≤ Output Level (*)	0.38148
–1.16dBFS ≤ Output Level < +0.53dBFS	0.06812
LM-LEVEL ≤ Output Level < –1.16dBFS	0.02548

* Output level is compared to the next sampling data

Table 33. ALC Limiter ATT Amount

2. ALC Recovery Operation

ALC recovery operation waits for the time set by WTM1-0 bits (Table 34) after completing ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 32) during the wait time, ALC recovery operation is executed. The VOL value is automatically incremented by the amount set by RGAIN2-0 bits (Table 35) up to the set reference level (Table 36) in every one sampling. When the VOL value exceeds the reference level (REF7-0), the VOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

ALC operations correspond to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to a microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of first recovery operation is set by RFST1-0 bits (Table 37).

WTM1 bit	WTM0 bit	Recovery Wait Time	
0	0	128/fs	(default)
0	1	256/fs	
1	0	512/fs	
1	1	1024/fs	

Table 34. ALC Recovery Operation Waiting Period

RGAIN2 bit	RGAIN1 bit	RGAIN0 bit	GAIN Step [dB]	GAIN Switching Timing	
0	0	0	0.00424	1/fs	(default)
0	0	1	0.00212	1/fs	
0	1	0	0.00106	1/fs	
0	1	1	0.00106	2/fs	
1	0	0	0.00106	4/fs	
1	0	1	0.00106	8/fs	
1	1	0	0.00106	16/fs	
1	1	1	0.00106	32/fs	

Table 35. ALC Recovery GAIN Step

REF7-0 bits	GAIN [dB]	Step	
F1H	+36.0	0.375 dB	
F0H	+35.625		
EFH	+35.25		
:	:		
E1H	+30.0		(default)
:	:		
92H	+0.375		
91H	0.0		
90H	–0.375		
:	:		
06H	–52.125		
05H	–52.5		
04H~00H	MUTE		

Table 36. Reference Level at ALC Recovery Operation

RFST1-0 bits	First Recovery Gain Step [dB]	
00	0.0032	(default)
01	0.0042	
10	0.0064	
11	0.0127	

Table 37. First Recovery Gain Step

3. Example of ALC Setting

Table 38 and Table 39 show the examples of the ALC setting for recording and playback path.

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
WTM1-0	Recovery waiting period	01	32ms	11	23.2ms
REF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
RGAIN2-0	Recovery GAIN	000	0.00424dB	011	0.00106dB (2/fs)
RFST1-0	Fast Recovery GAIN	11	0.0127dB	00	0.0032dB
ALCEQN	ALC EQ disable	0	Enable	0	Enable
ALC	ALC enable	1	Enable	1	Enable

Table 38. Example of the ALC Setting (Recording)

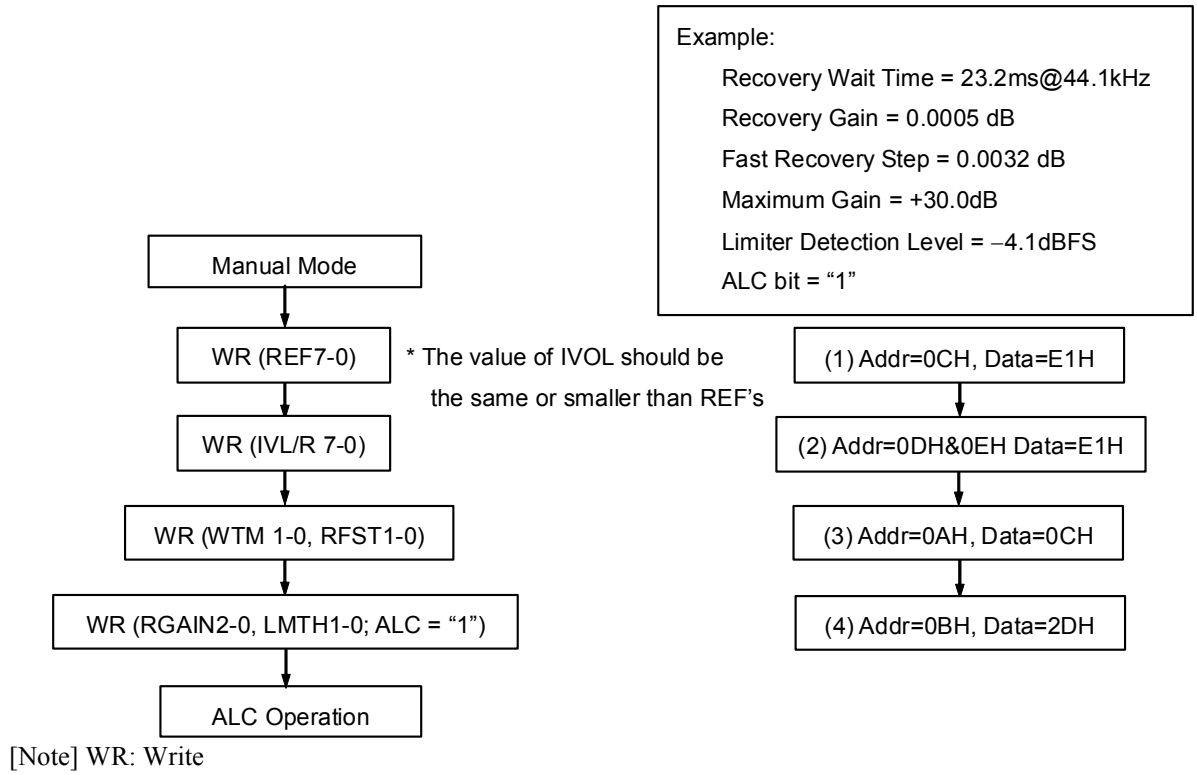
Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
WTM1-0	Recovery waiting period	01	32ms	11	23.2ms
REF7-0	Maximum gain at recovery operation	A1H	+6dB	A1H	+6dB
IVL7-0, IVR7-0	Gain of IVOL	91H	0dB	91H	0dB
RGAIN2-0	Recovery GAIN	000	0.00424dB	011	0.00106dB (2/fs)
RFST1-0	Fast Recovery GAIN	11	0.0127dB	00	0.0032dB
ALCEQN	ALC EQ disable	0	Enable	0	Enable
ALC	ALC enable	1	Enable	1	Enable

Table 39. Example of the ALC Setting (Playback)

4. Example of registers set-up sequence of ALC Operation

The following registers must not be changed during ALC operation. These bits must be changed after ALC operation is finished by ALC bit = “0”. The volume is changed by soft transition until manual mode starts after ALC bit is set to “0”.

LMTH1-0, WTM1-0, RGAIN 2-0, REF7-0 and RFST1-0 bits



[Note] WR: Write

Figure 37. Registers Set-up Sequence in ALC Operation (recording path)

■ Input Digital Volume (Manual Mode)

The input digital volume becomes manual mode by setting ALC bit = "0" when ADCPF bit ="1". This mode is used in the case shown below.

1. After exiting reset state, when setting up the registers for ALC operation (such as LMTH bit and etc.)
2. When the registers for ALC operation (Limiter period, Recovery period and etc.) are changed. For example; when the sampling frequency is changed.
3. When IVOL is used as a manual volume control.

IVL7-0 and IVR7-0 bits set the gain of the digital input volume (Table 40). Lch and Rch volumes are set individually by IVL7-0 and IVR7-0 bits when IVOLC bit = "0". IVL7-0 bits control both Lch and Rch volumes together when IVOLC bit = "1". PMPFIL bit must be "0" when changing the IVOLC bit setting. This volume has a soft transition function. Therefore no switching noise occurs during the transition. IVTM1-0 bits set the transition time between set values of IVL/R7-0 bits as either 236/fs, 944/fs, 1888/fs or 3776/fs (Table 41). When IVTM1-0 bits = "01", it takes 944/fs (21.4ms@fs=44.1kHz) from F1H(+36dB) to 05H(-52.5dB) when IVTM1-0 bits = "01". The volume is muted after transitioned to -72dB (208/fs=4.7ms @fs=44.1kHz) in the period set by IVTM1-0 bits when changing the volume from 05H (-52.5dB) to 00H (MUTE).

IVL7-0 bits IVR7-0 bits	GAIN [dB]	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		
E0H	+29.625		
:	:		
06H	–52.125		
05H	–52.5		
04H~00H	MUTE		

Table 40. Input Digital Volume Setting

IVTM1 bit	IVTM0 bit	Transition Time from F1H to 05H (IVL/R7-0 bits)				
		Setting	fs=8kHz	fs=44.1kHz	fs=96kHz	
0	0	236/fs	29.5ms	5.4ms	2.5ms	
0	1	944/fs	118ms	21.4ms	9.8ms	(default)
1	0	1888/fs	236ms	42.8ms	19.7ms	
1	1	3776/fs	472ms	85.6ms	39.3ms	

Table 41. Transition Time Setting of Input Digital Volume

If IVL7-0 or IVR7-0 bits are written during PMPFIL bit = "0", IVOL operation starts with the written values after PMPFIL bit is changed to "1".

■ Dynamic Range Control

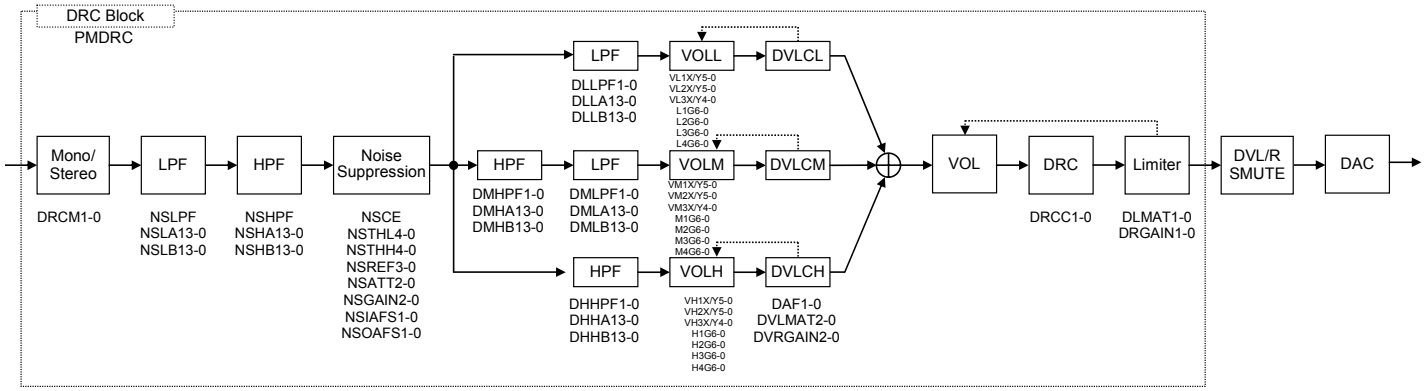


Figure 38. DRC Functions and Signal Path

DRCM1-0 bits select stereo or mono of DRC input data. In case of mono mode, the same data is input to both channels.

DRCM1 bit	DRCM0 bit	Lch	Rch	
0	0	L	R	(default)
0	1	L	L	
1	0	R	R	
1	1	N/A		

Table 42. DRC Stereo/Mono Select (N/A: Not available)

1. Noise Suppression Block

(1) Low Pass Filter (LPF)

This is composed with 1st order LPF. NSLA13-0 bits and NSLB13-0 bits set the coefficient of LPF. NSLPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when NSLPF bit = "0" or PMDRC bit = "0". The LPF starts operation 4/fs(max) after when NSLPF bit = "1" or PMDRC bit = "1" are set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting
LPF: NSLA[13:0] bits =A, NSLB[13:0] bits =B
(MSB=NSLA13, NSLB13; LSB=NSLA0, NSLB0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.05 (fc min = 2205Hz at 44.1kHz)

(2) High Pass Filter (HPF)

This is composed 1st order HPF. The coefficient of HPF is set by NSHA13-0 bits and NSHB13-0 bits. NSHPF bit controls ON/OFF of the HPF. When the HPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when NSHPF bit = "0" or PMDRC bit = "0". The HPF starts operation 4/fs(max) after when NSHPF bit = "1" or PMDRC bit = "1" are set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting
HPF: NSHA[13:0] bits =A, NSHB[13:0] bits =B
(MSB=NSHA13, NSHB13; LSB=NSHA0, NSHB0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.0001 (fc min = 4.41Hz at 44.1kHz)

(3) Noise Suppression

The Noise Suppression is enabled when NSCE bit (Noise suppression enable bit) = "1" during DRC operation (PMDRC bit = "1"). This function attenuates output signal level automatically when minute amount of the signal is input.

NSCE bit: Noise Suppression Enable
0: Disable (default)
1: Enable

(3-1) Noise Level Suppressing Operation

The output signal is suppressed when the input moving average level set by NSIAF1-0 bits (Table 43) is lower than "Noise Suppression Threshold Low Level" set by NSTHL4-0 bits (Table 44) during the normal operation.

This operation attenuats the volume automatically to the reference level set by NSREF3-0 bits (Table 45) with the soft transition of the attenuation speed set by NSATT2-0 bits (Table 46).

NSIAF1-0 bits	Moving Average Parameter				
		fs=8kHz	fs=16kHz	fs=44.1kHz	
00	256/fs	32ms	16ms	5.8ms	
01	512/fs	64ms	32ms	11.6ms	
10	1024/fs	128ms	64ms	23.2ms	(default)
11	2048/fs	256ms	128ms	46.4ms	

Table 43. Moving Average Parameter Setting at Noise Suppression Off

NSTHL4-0 bits	Noise Suppression Threshold Low Level [dB]	Step	
00H	–36.0	1.5dB	(default)
01H	–37.5		
02H	–39.0		
:	:		
10H	–60.0		
:	:		
1EH	–81.0		
1FH	–82.5		

Table 44. Noise Suppression Threshold Low Level

NSREF3-0 bits	GAIN [dB]	Step	
0H	–9	3dB	(default)
1H	–12		
2H	–15		
:	:		
AH	–39		
BH	–42		
CH	–45		
DH	–48		
EH	–51		
FH	–54		

Table 45. Reference Value Setting when Noise Suppression is ON

NSATT2 bit	NSATT1 bit	NSATT0 bit	ATT Speed			
			8kHz	16kHz	44.1kHz	
0	0	0	1.1dB/s	2.1dB/s	5.8dB/s	
0	0	1	2.1dB/s	4.2dB/s	11.7dB/s	(default)
0	1	0	4.2dB/s	8.5dB/s	23.4dB/s	
0	1	1	8.5dB/s	17.0dB/s	46.8dB/s	
1	0	0	17.0dB/s	33.9dB/s	93.5dB/s	
1	0	1	33.9dB/s	67.9dB/s	187.1dB/s	
1	1	0	N/A			
1	1	1				

Table 46. Noise Suppression ATT Speed Setting (N/A: Not available)

(3-2) Noise Suppression → Normal Operation

During noise suppressing operation, if the input moving average level set by NSOAF1-0 bits (Table 47) exceeds Noise Suppression Threshold High Level set by NSTHH4-0 bits (Table 48), the operation switches to normal operation from noise suppressing operation.

This recovery operation sets the volume automatically to 0dB with the soft transition of the recovery speed set by NSGAIN2-0 bits (Table 49).

NSOAF1-0 bits	Moving Average Parameter				
		fs=8kHz	fs=16kHz	fs=44.1kHz	
00	4/fs	0.5ms	0.3ms	0.1ms	
01	8/fs	1.0ms	0.5ms	0.2ms	
10	16/fs	2.0ms	1.0ms	0.4ms	(default)
11	32/fs	4.0ms	2.0ms	0.7ms	

Table 47. Moving Average Parameter Setting at Noise Suppression On

NSTHH4-0 bits	Noise Suppression Threshold High Level [dB]	Step	
00H	–36.0	1.5dB	(default)
01H	–37.5		
02H	–39.0		
:	:		
10H	–60.0		
:	:		
1EH	–81.0		
1FH	–82.5		

Table 48. Noise Suppression Threshold High Level

NSGAIN2 bit	NSGAIN1 bit	NSGAIN0 bit	Recovery Speed			
			8kHz	16kHz	44.1kHz	
0	0	0	0.3dB/ms	0.5dB/ms	1.5dB/ms	
0	0	1	0.5dB/ms	1.1dB/ms	3.0dB/ms	(default)
0	1	0	1.1dB/ms	2.2dB/ms	6.0dB/ms	
0	1	1	2.2dB/ms	4.4dB/ms	12.2dB/ms	
1	0	0	4.5dB/ms	9.0dB/ms	24.7dB/ms	
1	0	1	N/A			
1	1	0				
1	1	1				

Table 49. Recovery Speed Setting from Noise Suppression to Normal Operation (N/A: Not available)

2. Dynamic Volume Control Block

The AK4954A has the dynamic volume control (DVLC) circuits before DRC. DVLC divides frequency range into three band (Low, Middle and High) and controls independently. To set characteristics of the DVLC circuit around flat, it is recommended that the cutoff frequencies of the LPF for Low Frequency Range is set to the same value of cutoff frequency of HPF for Middle Frequency Range, and the cutoff frequency of LPF for Middle Frequency Range is set to the same value of cutoff frequency of HPF for High Frequency Range when using first order LPF and HFP. When using second order filters, the cutoff frequency of the LPF for Low Frequency Range should be set to the value which is four times than the HPF for Middle Frequency Range, and the cutoff frequency of the LPF for Middle Frequency Range should be set to the value which is four times than the HPF for High Frequency Range.

(1) Low Frequency Range

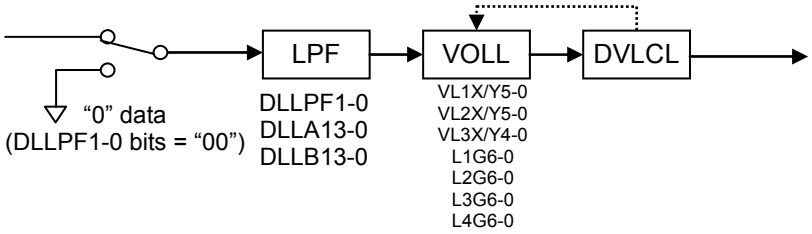


Figure 39. DVLC Functions and Signal Path for Low Frequency Range

(1-1) Low Pass Filter (LPF)

This is composed with 1st or 2nd order LPF. DLLA13-0 bits and DLLB13-0 bits set the coefficient of LPF. DLLPF1-0 bits controls ON/OFF of the LPF. When the LPF is OFF, the audio data does not pass this block. The coefficient must be set when DLLPF1-0 bits = "00" or PMDRC bit = "0". The LPF starts operation 4/fs(max) after when DLLPF1-0 bits = "01" or "10" and PMDRC bit = "1" are set.

DLLPF1 bit	DLLPF0 bit	Mode	
0	0	OFF ("0" data)	(default)
0	1	1st order LPF	
1	0	2nd order LPF	
1	1	N/A	

Table 50. DLLPF Mode Setting (N/A: Not available)

fs: Sampling frequency
fc: Cut-off frequency

Register setting
LPF: DLLA[13:0] bits =A, DLLB[13:0] bits =B
(MSB=DLLA13, DLLB13; LSB=DLLA0, DLLB0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function (1st order)

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

Transfer function (2nd order)

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}} \times A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.002 (fc min = 88Hz at 44.1kHz)

(1-2) Dynamic Volume Control Curve

The inflection points of the DVLC curve is set by three coordinate values (VL1X5-0, VL1Y5-0, VL2X5-0, VL2Y5-0, VL3X4-0 and VL3Y4-0 bits). The setting of three inflection points are calculated the values of ($X1_L$, $Y1_L$), ($X2_L$, $Y2_L$), ($X3_L$, $Y3_L$) in dB. The inflection points should be set in such a way that VL1X ≤ VL2X ≤ VL3X, VL1Y ≤ VL2Y ≤ VL3Y. And the each slope is set by L1G6-0, L2G6-0, L3G6-0 and L4G6-0 bits. $X4_L$ is fixed full-scale, $Y4_L$ is calculated by the L4G value. The initial value of the DVLC gain is set by the L1G.

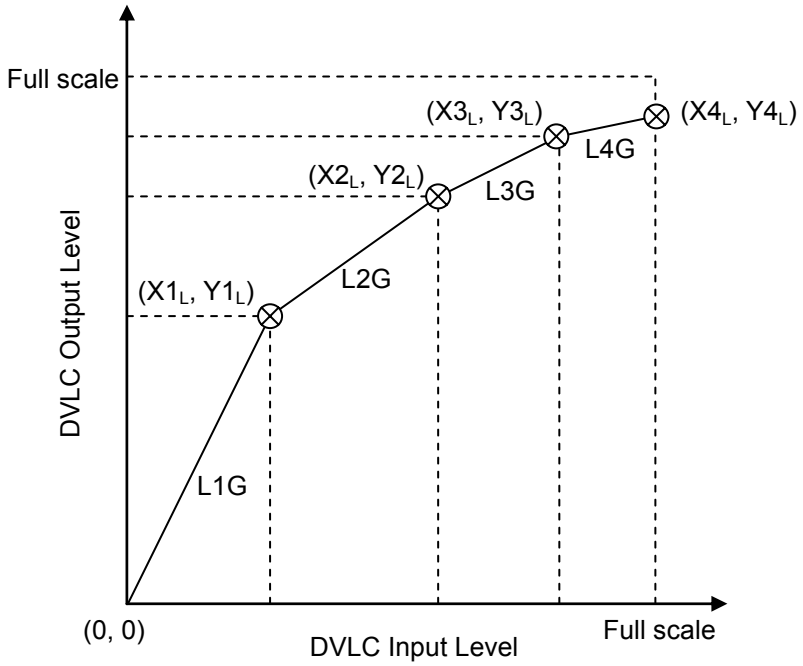


Figure 40. DVLC Curve for Low Frequency Range

VL1X/Y5-0 bits VL2X/Y5-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	−1.5		
02H	−3.0		
:	:		
2EH	−69.0		
2FH	−70.5		
30H	N/A	N/A	
:	:		
3FH	N/A		

Table 51. DVLC Point Setting for X/Y1, X/Y2 (N/A: Not available)

VL3X/Y4-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	–1.5		
02H	–3.0		
:	:		
1EH	–45.0		
1FH	–46.5		

Table 52. DVLC Point Setting for X/Y3

Slope Setting

$$L1G = \frac{Y1_L}{X1_L} \times 16, \quad L2G = \frac{(Y2_L - Y1_L)}{(X2_L - X1_L)} \times 16,$$

$$L3G = \frac{(Y3_L - Y2_L)}{(X3_L - X2_L)} \times 16, \quad L4G = \frac{(Y4_L - Y3_L)}{(X4_L - X3_L)} \times 16,$$

The results calculated by the equations above should be rounded off to integer. These integers are slope data. $X1/2/3_L$ and $Y1/2/3_L$ values must be set to keep the Slope Data 127 or less (Gain ≤ 18dB).

L1G6-0 bits, L2G6-0 bits, L3G6-0 bits, L4G6-0 bits	Slope Data	Gain [dB] (20 log (Slope Data / 16))	
00H	0	-∞	(default)
01H	1	-24.08	
02H	2	-18.06	
:	:	:	
10H	16	0	
:	:	:	
7EH	126	17.93	
7FH	127	17.99	

Table 53. DVLC Slope Setting for Low Frequency Range

(2) Middle Frequency Range

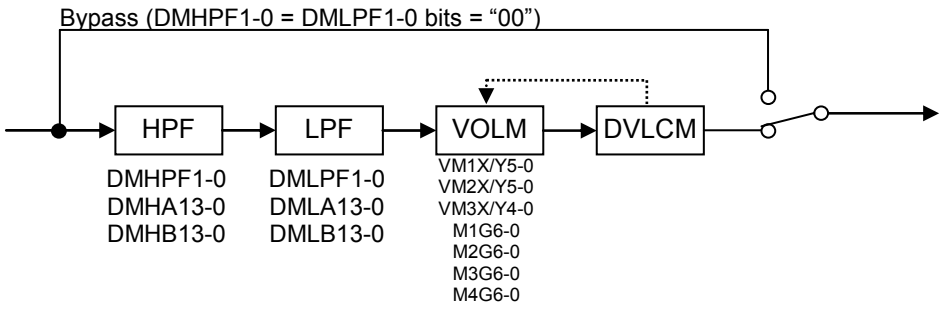


Figure 41. DVLC Functions and Signal Path for Middle Frequency Range

(2-1) High Pass Filter (HPF)

This is composed with 1st or 2nd order HPF. The coefficient of HPF is set by DMHA13-0 bits and DMHB13-0 bits. HPF bit controls ON/OFF of the HPF. When the HPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when DMHPF1-0 bits = "00" or PMDRC bit = "0". The HPF starts operation 4/fs(max) after when DMHPF1-0 bits = "01" or "10" and PMDRC bit = "1" are set.

DMHPF1 bit	DMHPF0 bit	Mode	
0	0	Bypass	(default)
0	1	1st order HPF	
1	0	2nd order HPF	
1	1	N/A	

Table 54. DMHPF Mode Setting (N/A: Not available)

fs: Sampling frequency
fc: Cut-off frequency

Register setting
HPF: DMHA[13:0] bits =A, DMHB[13:0] bits =B
(MSB=DMHA13, DMHB13; LSB=DMHA0, DMHB0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function (1st order)

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

Transfer function (2nd order)

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}} \times A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.0001 (fc min = 4.41Hz at 44.1kHz)

(2-2) Low Pass Filter (LPF)

This is composed with 1st or 2nd order LPF. DMLA13-0 bits and DMLB13-0 bits set the coefficient of LPF. DMLPF1-0 bits controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when DMLPF1-0 bits = "00" or PMDRC bit = "0". The LPF starts operation 4/fs(max) after when DMLPF1-0 bits = "01" or "10" and PMDRC bit = "1" are set.

DMLPF1 bit	DMLPF0 bit	Mode	
0	0	Bypass	(default)
0	1	1st order LPF	
1	0	2nd order LPF	
1	1	N/A	

Table 55. DMLPF Mode Setting (N/A: Not available)

fs: Sampling frequency
fc: Cut-off frequency

Register setting
LPF: DMLA[13:0] bits =A, DMLB[13:0] bits =B
(MSB=DMLA13, DMLB13; LSB=DMLA0, DMLB0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function (1st order)

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

Transfer function (2nd order)

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}} \times A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
$fc/fs \geq 0.05$ (fc min = 2205Hz at 44.1kHz)

(2-3) Dynamic Volume Control Curve

The inflection points of the DVLC curve is set by three coordinate values (VM1X5-0, VM1Y5-0, VM2X5-0, VM2Y5-0, VM3X4-0 and VM3Y4-0 bits). The setting of three inflection points are calculated the values of ($X1_M$, $Y1_M$), ($X2_M$, $Y2_M$), ($X3_M$, $Y3_M$) in dB. The inflection points should be set in such a way that VM1X ≤ VM2X ≤ VM3X, VM1Y ≤ VM2Y ≤ VM3Y. And the each slope is set by M1G6-0, M2G6-0, M3G6-0 and M4G6-0 bits. $X4_M$ is fixed full-scale, $Y4_M$ is calculated by the M4G value. The initial value of the DVLC gain is set by the M1G. When the HPF and LPF is bypass (DMHPF1-0 = DMLPF1-0 bits = "00"), the audio data passes this block by 0dB gain.

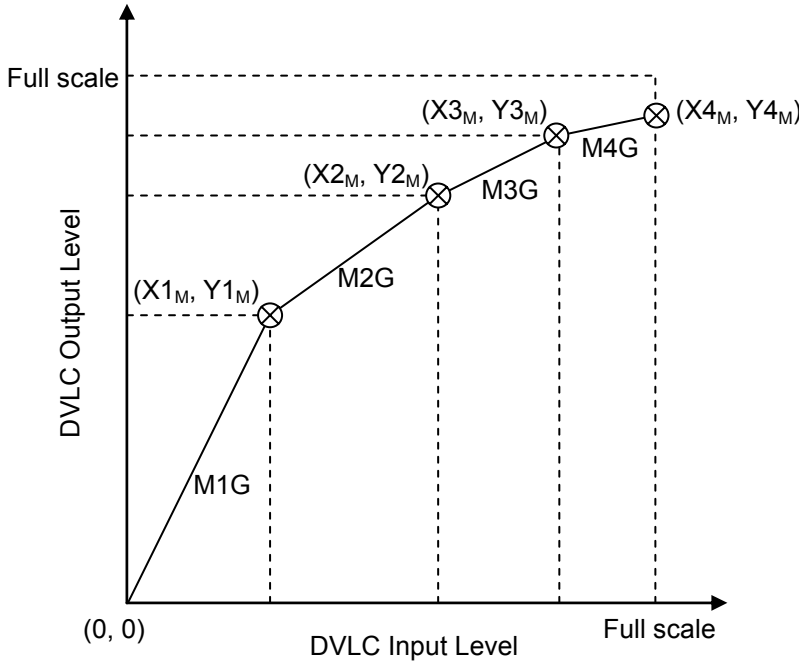


Figure 42. DVLC Curve for Middle Frequency Range

VM1X/Y5-0 bits VM2X/Y5-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	–1.5		
02H	–3.0		
:	:		
2EH	–69.0		
2FH	–70.5		
30H	N/A	N/A	
:	:		
3FH	N/A		

Table 56. DVLC Point Setting for X/Y1, X/Y2 (N/A: Not available)

VM3X/Y4-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	–1.5		
02H	–3.0		
:	:		
1EH	–45.0		
1FH	–46.5		

Table 57. DVLC Point Setting for X/Y3

Slope Setting

$$M1G = \frac{Y1_M}{X1_M} \times 16, \quad M2G = \frac{(Y2_M - Y1_M)}{(X2_M - X1_M)} \times 16,$$

$$M3G = \frac{(Y3_M - Y2_M)}{(X3_M - X2_M)} \times 16, \quad M4G = \frac{(Y4_M - Y3_M)}{(X4_M - X3_M)} \times 16,$$

The results calculated by the equations above should be rounded off to integer. These integers are slope data. $X1/2/3_M$ and $Y1/2/3_M$ values must be set to keep the Slope Data 127 or less (Gain ≤ 18dB).

M1G6-0 bits, M2G6-0 bits, M3G6-0 bits, M4G6-0 bits	Slope Data	Gain [dB] (20 log (Slope Data / 16))	
00H	0	-∞	(default)
01H	1	-24.08	
02H	2	-18.06	
:	:	:	
10H	16	0	
:	:	:	
7EH	126	17.93	
7FH	127	17.99	

Table 58. DVLC Slope Setting for Middle Frequency Range

(3) High Frequency Range

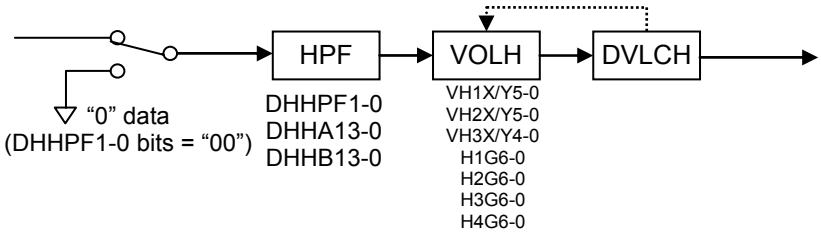


Figure 43. DVLC Functions and Signal Path for High Frequency Range

(3-1) High Pass Filter (HPF)

This is composed with 1st or 2nd order HPF. The coefficient of HPF is set by DHHA13-0 bits and DHHB13-0 bits. DHHPF1-0 bits control ON/OFF of the HPF. When the HPF is OFF, the audio data does not pass this block. The coefficient must be set when DHHPF1-0 bits = "00" or PMDRC bit = "0". The HPF starts operation 4/fs(max) after when DHHPF1-0 bits = "01" or "10" and PMDRC bit = "1" are set.

DHHPF1 bit	DHHPF0 bit	Mode	
0	0	OFF ("0" data)	(default)
0	1	1st order HPF	
1	0	2nd order HPF	
1	1	N/A	

Table 59. DHHPF Mode Setting (N/A: Not available)

fs: Sampling frequency
fc: Cut-off frequency

Register setting
HPF: DHHA[13:0] bits =A, DHHB[13:0] bits =B
(MSB=DHHA13, DMHB13; LSB=DHHA0, DHHB0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function (1st order)

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

Transfer function (2nd order)

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}} \times A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.0001 (fc min = 4.41Hz at 44.1kHz)

(3-2) Dynamic Volume Control Curve

The inflection points of the DVLC curve is set by three coordinate values (VH1X5-0, VH1Y5-0, VH2X5-0, VH2Y5-0, VH3X4-0 and VH3Y4-0 bits). The setting of three inflection points are calculated the values of ($X1_H$, $Y1_H$), ($X2_H$, $Y2H_H$), ($X3_H$, $Y3_H$) in dB. The inflection points should be set in such a way that VH1X ≤ VH2X ≤ VH3X, VH1Y ≤ VH2Y ≤ VH3Y. And the each slope is set by H1G6-0, H2G6-0, H3G6-0 and H4G6-0 bits. $X4_H$ is fixed full-scale, $Y4_H$ is calculated by the H4G value. The initial value of the DVLC gain is set by the H1G.

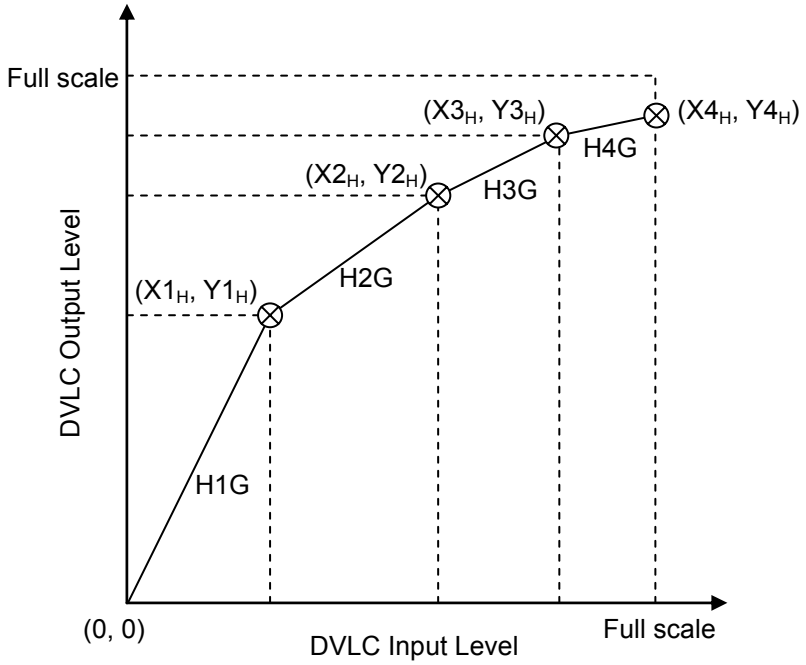


Figure 44. DVLC Curve for High Frequency Range

VH1X/Y5-0 bits VH2X/Y5-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	–1.5		
02H	–3.0		
:	:		
2EH	–69.0		
2FH	–70.5		
30H	N/A	N/A	
:	:		
3FH	N/A		

Table 60. DVLC Point Setting for X/Y1, X/Y2 (N/A: Not available)

VH3X/Y4-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	–1.5		
02H	–3.0		
:	:		
1EH	–45.0		
1FH	–46.5		

Table 61. DVLC Point Setting for X/Y3

Slope Setting

$$H1G = \frac{Y1_H}{X1_H} \times 16, \quad H2G = \frac{(Y2_H - Y1_H)}{(X2_H - X1_H)} \times 16,$$

$$H3G = \frac{(Y3_H - Y2_H)}{(X3_H - X2_H)} \times 16, \quad H4G = \frac{(Y4_H - Y3_H)}{(X4_H - X3_H)} \times 16$$

The results calculated by the equations above should be rounded off to integer. These integers are slope data. $X1/2/3_H$ and $Y1/2/3_H$ values must be set to keep the Slope Data 127 or less (Gain ≤ 18dB).

H1G6-0 bits, H2G6-0 bits, H3G6-0 bits, H4G6-0 bits	Slope Data	Gain [dB] (20 log (Slope Data / 16))	
00H	0	-∞	(default)
01H	1	-24.08	
02H	2	-18.06	
:	:	:	
10H	16	0	
:	:	:	
7EH	126	17.93	
7FH	127	17.99	

Table 62. DVLC Slope Setting for High Frequency Range

(4) Dynamic Volume Control

The DVLC automatically controls the volume at the attenuation speed set by DVLMAT2-0 bits (Table 64) or the recovery speed set by DVRGAIN2-0 bits (Table 65) in such a way that the input moving average level set by DAF1-0 bits (Table 63) is reached the output level of the DVLC curve set by each frequency range.

DAF1-0 bits	Moving Average Parameter				
		fs=8kHz	fs=16kHz	fs=44.1kHz	
00	256/fs	32ms	16ms	5.8ms	
01	512/fs	64ms	32ms	11.6ms	
10	1024/fs	128ms	64ms	23.2ms	
11	2048/fs	256ms	128ms	46.4ms	(default)

Table 63. DVLC Moving Average Parameter Setting

DVLMAT2 bit	DVLMAT1 bit	DVLMAT0 bit	ATT Speed			
			8kHz	16kHz	44.1kHz	
0	0	0	1.1dB/s	2.1dB/s	5.8dB/s	
0	0	1	2.1dB/s	4.2dB/s	11.7dB/s	
0	1	0	4.2dB/s	8.5dB/s	23.4dB/s	
0	1	1	8.5dB/s	17.0dB/s	46.8dB/s	(default)
1	0	0	17.0dB/s	33.9dB/s	93.5dB/s	
1	0	1	33.9dB/s	67.9dB/s	187.1dB/s	
1	1	0	67.9dB/s	135.8dB/s	374.3dB/s	
1	1	1	N/A			

Table 64. DVLC ATT Speed Setting (N/A: Not available)

DVRGAIN2 bit	DVRGAIN1 bit	DVRGAIN0 bit	Recovery Speed			
			8kHz	16kHz	44.1kHz	
0	0	0	0.07dB/s	0.13dB/s	0.37dB/s	
0	0	1	0.13dB/s	0.27dB/s	0.73dB/s	
0	1	0	0.27dB/s	0.53dB/s	1.46dB/s	
0	1	1	0.53dB/s	1.06dB/s	2.92dB/s	(default)
1	0	0	1.06dB/s	2.12dB/s	5.84dB/s	
1	0	1	2.12dB/s	4.24dB/s	11.7dB/s	
1	1	0	4.24dB/s	8.48dB/s	23.4dB/s	
1	1	1	N/A			

Table 65. DVLC Recovery Speed Setting (N/A: Not available)

3. Dynamic Range Control Block

The AK4954A has the dynamic range control (DRC) circuits. The compression level is selected in three levels and set by DRCC1-0 bits (Table 66).

When the DRC is OFF (DRCC1-0 bits = "00"), the audio data passes this block by 0dB gain. However limiter and recovery operation is always ON. The compression level must be set when PMDRC bit = "0".

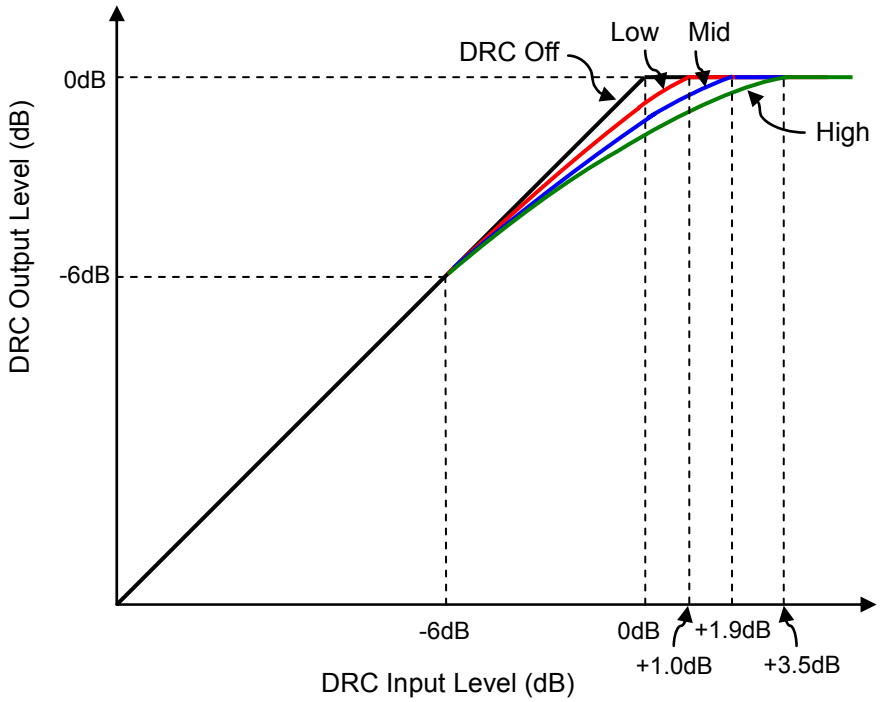


Figure 45. DRC Gain Curve

DRCC1 bit	DRCC0 bit	Compression Level	
0	0	OFF	(default)
0	1	Low	
1	0	Middle	
1	1	High	

Table 66. DRC Compression Level Setting

1. DRC Limiter Operation

During the DRC limiter operation, when the output level of DRC exceeds full-scale, the DRC volume are attenuated automatically with the soft transition in the attenuation speed set by DLMAT2-0 bits (Table 67).

DLMAT2 bit	DLMAT1 bit	DLMAT0 bit	ATT Speed			
			8kHz	16kHz	44.1kHz	
0	0	0	0.1dB/ms	0.3dB/ms	0.7dB/ms	(default)
0	0	1	0.3dB/ms	0.5dB/ms	1.5dB/ms	
0	1	0	0.5dB/ms	1.1dB/ms	3.0dB/ms	
0	1	1	1.1dB/ms	2.2dB/ms	6.0dB/ms	
1	0	0	2.2dB/ms	4.4dB/ms	12.2dB/ms	
1	0	1	4.5dB/ms	9.0dB/ms	24.7dB/ms	
1	1	0	N/A			
1	1	1				

Table 67. DRC ATT Speed Setting (N/A: Not available)

2. DRC Recovery Operation

During the DRC recovery operation, when the DRC volume reaches 0dB or the output level of DRC exceeds limiter detection level, the DRC volume are set automatically with the soft transition in the recovery speed set by DRGAIN1-0 bits (Table 68).

DRGAIN1 bit	DRGAIN0 bit	Recovery Speed			
		8kHz	16kHz	44.1kHz	
0	0	1.1dB/s	2.1dB/s	5.9dB/s	(default)
0	1	2.1dB/s	4.2dB/s	11.7dB/s	
1	0	4.2dB/s	8.5dB/s	23.4dB/s	
1	1	8.5dB/s	17.0dB/s	46.7dB/s	

Table 68. DRC Recovery Speed Setting

■ Output Digital Volume

The AK4954A has a digital output volume (128 levels, 0.5dB step, Mute). The volume can be set by the DVL7-0 and DVR7-0 bits. The volume is included in front of a DAC block. The input data of DAC is changed from +6 to –68.5dB or MUTE. When the DVOLC bit = "1", the DVL7-0 bits control both Lch and Rch attenuation levels. When the DVOLC bit = "0", the DVL7-0 bits control Lch level and DVR7-0 bits control Rch level. This volume has soft transition function. Therefore no switching noise occurs during the transition. The DVTM1-0 bits set the transition time between set values of DVL/R7-0 bits (from 00H to 90H) as either 144/fs, 288/fs or 576/fs (Table 70). When DVTM1-0 bits = "01", it takes 576/fs (13ms@fs=44.1kHz) from 00H (+6dB) to 90H (MUTE).

DVL7-0 bits DVR7-0 bits	Gain	Step	
00H	+6.0dB	0.5dB	
01H	+5.5dB		
02H	+5.0dB		
:	:		
0CH	0dB		(default)
:	:		
8EH	-65.0dB		
8FH	-65.5dB		
90H~FFH	Mute (- ∞)		

Table 69. Output Digital Volume2 Setting

DVTM1 bit	DVTM0 bit	Transition Time between DVL/R7-0 bits = 00H and 90H				
		Setting	fs=8kHz	fs=44.1kHz	fs=96kHz	
0	0	144/fs	18ms	3.3ms	1.5ms	
0	1	288/fs	36ms	6.5ms	3.0ms	
1	0	576/fs	72ms	13ms	6.0ms	(default)
1	1	N/A				

Table 70. Transition Time Setting of Output Digital Volume2 (N/A: Not available)

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is set "1", the output signal is attenuated by -∞ ("0") during the cycle set by DVTM1-0 bits. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the value set by DVL/R7-0 bits from -∞ during the cycle set by DVTM1-0 bits. If the soft mute is cancelled within the cycle set by DVTM1-0 bits after starting the operation, the attenuation is discontinued and returned to the level set by DVL/R7-0 bits. The soft mute is effective for changing the signal source without stopping the signal transaction (Figure 46)

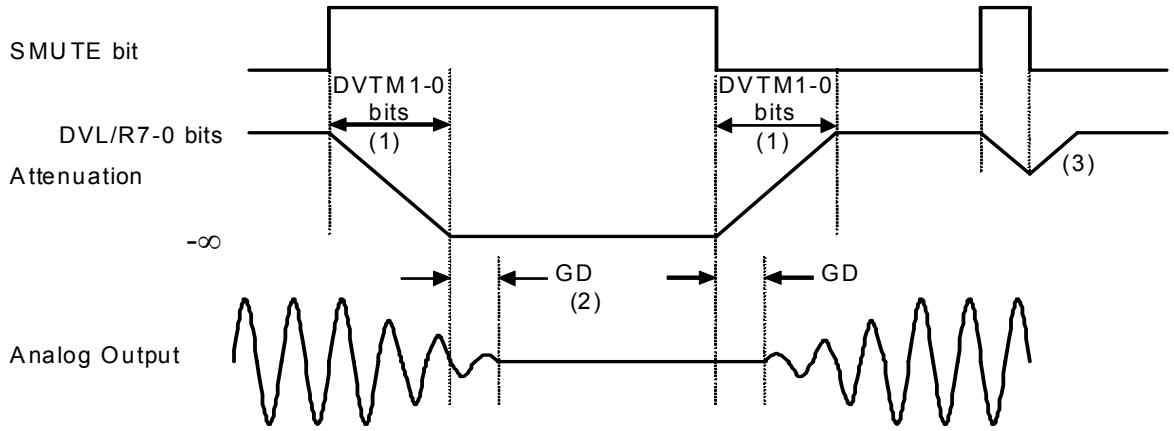


Figure 46. Soft Mute Function

(1) The input signal is attenuated by –∞ ("0") during the cycle set by DVTM1-0 bits.
(2) Analog output corresponding to digital input has group delay (GD).
(3) If soft mute is cancelled within the cycle set by DVTM1-0 bits after starting the operation, the attenuation is discounted and returned to the value set by DVL/R7-0 bits within the same cycle.

■ Mixing Setting of Digital Block

The DAC output signal is mixed and output as (L+R)/2 when MONO bit = "1". Output signal from the HPL/HPR or LOUT/ROUT pins is monaural.

MONO bit	Lch	Rch	
0	L	R	(default)
1	(L+R)/2	(L+R)/2	

Table 71. DAC Output Monaural Mixing

■ BEEP Generating Circuit

The AK4954A integrates a BEPP generating circuit. When PMSL bit = "1", the speaker amplifier outputs the BEEP by setting PMBP bit = "1", and the Headphone amplifier outputs the BEEP by setting PMBP bit = "1" when PMHPL bit or PMHPR bit = "1".

When PMDAC bit = "1" and PMHPL bit or PMHPR bit = "1", switching noise of connection between the BEEP generating circuit and headphone amplifier can be suppressed by soft transition. The transition time of ON/OFF switching is set by PTS1-0 bits. Soft transition Enable/Disable is controlled by MOFF bit. When this bit is "1", soft transition is disabled and the headphone is switched ON/OFF immediately.

PTS1 bit	PTS0 bit	ON/OFF Time						
		8kHz ≤ fs ≤ 24kHz		24kHz < fs ≤ 48kHz		48kHz < fs ≤ 96kHz		
0	0	64/fs	2.7 ~ 8ms	128/fs	2.7 ~ 5.3ms	256/fs	2.7 ~ 5.3ms	
0	1	128/fs	5.3 ~ 16ms	256/fs	5.3 ~ 10.7ms	512/fs	5.3 ~ 10.7ms	(default)
1	0	256/fs	10.7 ~ 32ms	512/fs	10.7 ~ 21.3ms	1024/fs	10.7 ~ 21.3ms	
1	1	512/fs	21.3 ~ 64ms	1024/fs	21.3 ~ 42.7ms	2048/fs	21.3 ~ 42.7ms	

Table 72. BEEP (Headphone Amplifier) ON/OFF Transition Time

After outputting the signal during the time set by BPON7-0 bits, the AK4954A stops the output signal during the time set by BPOFF7-0 bits (Figure 47). The repeat count is set by BPTM6-0 bits, and the output level is set by BPLVL4-0 bits. When BPCNT bit is "0", if BPOUT bit is written "1", the AK4954A outputs the beep for the times of repeat count. When the output is finished, BPOUT bit is set to "0" automatically. When BPCNT bit is set to "1", it outputs beep signals incessantly regardless of repeat count, on-time nor off-time. The output frequency is set by BPFR1-0 bits.

< Setting parameter >

1) Output Frequency (Table 73)
2) ON Time (Table 74)
3) OFF Time (Table 75)
4) Repeat Count (Table 76)
5) Output Level (Table 77)

*** BPFR1-0, BPON7-0, BPOFF7-0, BPTM6-0 and BPLVL4-0 bits should be set when BPOUT =BPCNT = "0".**

*** BPCNT bit is given priority in BPOUT bit. When BPOUT bit is set to "1", if BPCNT bit is set to "0", BPOUT bit is set to "0" forcibly.**

*** When stopping the BEEP outputs by changing BPCNT bit to "0" from "1", writing to BPOUT and BPCNT bits are inhibited for 10ms. When BEEP is output by setting BPCNT bit = "1", writing to BPOUT and BPCNT bits are inhibited for 10ms after BPOUT bit is changed to "0" or BEEP outputs are finished (ON/OFF time and the number of times set by repeated time).**

*** When stopping the BEEP output and outputting the input signal from DAC, put BPCNT bit "0" first before setting PMBP bit = "0" and PMDAC bit = "1". Writing PMBP bit = "0" is prohibited during BPCNT bit = "1".**

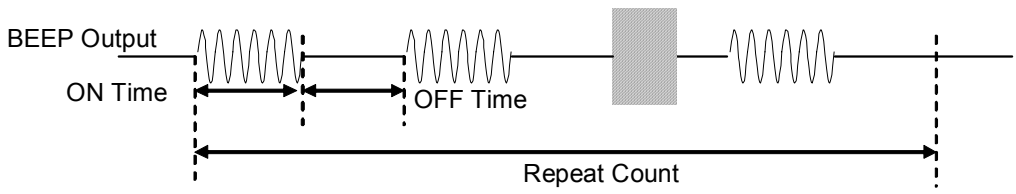


Figure 47. BEEP Output

BPFR1-0 bits	Output frequency of BEEP Generator [Hz]			
	FS1-0 bits = "00"	FS1-0 bits = "01"	FS1-0 bits = "10", "11"	
00	4000	4009	4000	(default)
01	2000	2005	2000	
10	1306	1297	1297	
11	800	802	800	

Table 73. Beep Output Frequency

BPON7-0 bits	ON Time of BEEP Generator [msec]		Step[msec]		
	fs=48kHz (Note 45)	fs=44.1kHz (Note 46)	fs=48kHz (Note 45)	fs=44.1kHz (Note 46)	
0H	8.0	7.98	8.0	7.98	(default)
1H	16.0	15.96			
2H	24.0	23.95			
3H	32.0	31.93			
:	:	:			
FDH	2032	2027.3			
FEH	2040	2035.3			
FFH	2048	2043.4			

Note 45. When the sampling frequency is 8kHz, 16kHz, 32kHz, 48kHz, 64kHz or 96kHz.
Note 46. When the sampling frequency is 11.025kHz, 22.05kHz, 44.1kHz or 88.2kHz.

Table 74. Beep Output ON-time

BPOFF7-0 bits	OFF Time of BEEP Generator [msec]		Step[msec]		
	fs = 48kHz (Note 45)	fs = 44.1kHz (Note 46)	fs = 48kHz (Note 45)	fs = 44.1kHz (Note 46)	
0H	8.0	7.98	8.0	7.98	(default)
1H	16.0	15.96			
2H	24.0	23.95			
3H	32.0	31.93			
:	:	:			
FDH	2032	2027.3			
FEH	2040	2035.3			
FFH	2048	2043.4			

Note 45. When the sampling frequency is 8kHz, 16kHz, 32kHz, 48kHz, 64kHz or 96kHz.
Note 46. When the sampling frequency is 11.025kHz, 22.05kHz, 44.1kHz or 88.2kHz.

Table 75. Beep Output OFF-time

BPTM6-0 bits	Repeat Count	
0H	1	(default)
1H	2	
2H	3	
:	:	
7DH	126	
7EH	127	
7FH	128	

Table 76. Beep Output Repeat Count

BPLVL4-0 bits	Beep Output Level	STEP	
0H	0dB	3dB	(default)
1H	–3dB		
2H	–6dB		
:	:		
12H	–54dB		
13H	–57dB		
14H	–60dB		

Note 47. Beep output amplitude in 0dB setting is 1.5Vpp @16Ω from the headphone amplifier, 2.8Vpp @8Ω (SLG1-0 bits = "00") from the speaker amplifier, and 1.4Vpp @10kΩ (SLG1-0 bits= "00") from stereo line output.

Table 77. Beep Output Level

■ Charge Pump Circuit

The internal charge pump circuit generates negative voltage (VEE) from AVDD voltage. The VEE voltage is used for the headphone amplifier and the speaker amplifier in low voltage mode (LSV bit = "1"). The charge pump circuit starts operation when PMHPL or PMHPR bit = "1", or when LSV bit = PMSPK bit = "1". PMVCM bit must be set "1" to power up the charge pump circuit.

The power-up time of the charge pump circuit is 11ms (max). The headphone amplifier and speaker amplifier will be powered up after the charge pump circuit is powered up (when PMHPL or PMHPR bit = "1", or LSV bit = PMSPK bit = "1"). The operating frequency of the charge pump circuit is dependent on the sampling frequency.

■ Headphone Amplifier (HPL/HPR pins)

The positive voltage of the headphone amplifier uses the power supply to the DVDD pin, therefore 150mA of the maximum power supply capacity is needed. The internal charge pump circuit generates negative voltage (VEE) from AVDD voltage. The headphone amplifier output is single-ended and centered around on VSS (0V). Therefore, the capacitor for AC-coupling can be removed. The minimum load resistance is 16Ω.

<External Circuit of Headphone Amplifier>

An oscillation prevention circuit (0.22μF±20% capacitor and 33Ω±20% resistor) should be put because it has the possibility that Headphone Amplifier oscillates in type of headphone.

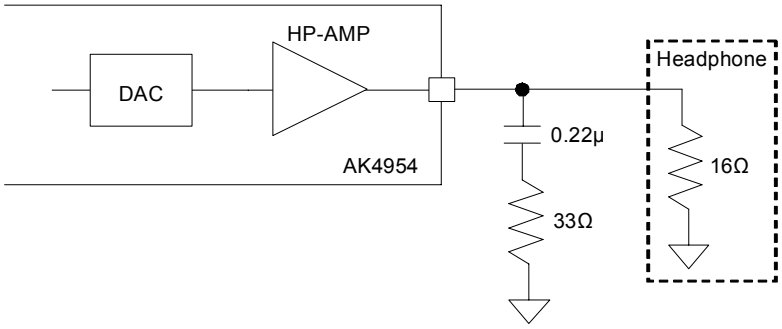


Figure 48. External Circuit of Headphone

When HPZ bit = "0" and PMHPL, PMHPR bits = "1", headphone outputs are in normal operation.

By setting PMHPL and PMHPR bits = "0", the headphone-amps are powered-down completely. At that time, the HPL and HPR pins go to VSS voltage via the internal pulled-down resistor. The pulled-down resistor is 10Ω (typ). Crosstalk can be reduced by bringing the HPL and HPR pins to Hi-Z state when it occurs on the path from speaker output to headphone output by enabling the speaker output in this pulled-down status of the HPL and HPR pins. The HPL and HPR pins become Hi-Z state by setting HPZ bit to "1" when PMHPL and PMHPR bit = "0".

The power-up time of the headphone amplifiers is 30ms (max.), and power-down is executed immediately.

PMVCM bit	PMHPL/R bits	HPZ bit	Mode	HPL/R pins	
x	0	0	Power-down & Mute	Pull-down by 10Ω (typ)	(default)
x	0	1	Power-down	Hi-Z	
1	1	0	Normal Operation	Normal Operation	
1	1	1	N/A	N/A	

Table 78. Headphone Output Status (x: Don't care, N/A: Not available)

<Low-power Consumption Mode>

LPDA bit controls the operation mode of the DAC and Headphone amplifier (Table 79).

LPDA bit	Mode	Power Consumption (DAC → Headphone out)	S/N (A-weighted)	
0	Normal	8.5mW	100dB	(default)
1	Low-power Consumption	6.2mW	99dB	

Table 79. DAC + Headphone Operation Mode

■ Speaker Output (SPP/SPN pins, LOSEL bit = "0")

The DAC output signal is input to the speaker amplifier as [(L+R)/2]. The speaker amplifier is mono and BTL output. The gain is set by SLG1-0 bits. Output level depends on SVDD voltage and SLG1-0 bits. The AK4954A has a low voltage mode (LSV bit = "1") which the speaker amplifier can be operated by SVDD= 0.9V ~ 2.0V. In low voltage mode, the negative power which is generated by the charge pump circuit using the voltage from the AVDD pin is used. This negative power is not used in normal voltage mode (LSV bit = "0", SVDD=1.8V~5.5V). In low voltage mode, SLG1-0 bits must be set to "00" and the DAC output level should be set to lower level by setting digital volume so that the speaker amplifier outputs is suppressed to lower level and output signal is not clipped.

SLG1-0 bits	Gain	
00	4.26 dB	(default)
01	6.26 dB	
10	8.26 dB	
11	10.26 dB	

Table 80. SPK Amplifier Gain (LOSEL bit = "0")

SLG1-0 bits	SPK Amplifier Output (DAC Input=0dBFS, AVDD=SVDD=3.3V)
00	3.37Vpp
01	4.23Vpp (Note 48)
10	5.33Vpp (Note 48)
11	6.71Vpp (Note 48)

Note 48. The output level is calculated by assuming that output signal is not clipped. In the actual case, the output signal may be clipped when DAC outputs 0dBFS signal. The DAC output level should be set to lower level by setting digital volume so that the speaker amplifier output level is 4.0Vpp or less, and the output signal is not clipped.

Table 81. SPK Amplifier Output Level

< Speaker Amplifier Control Sequence >

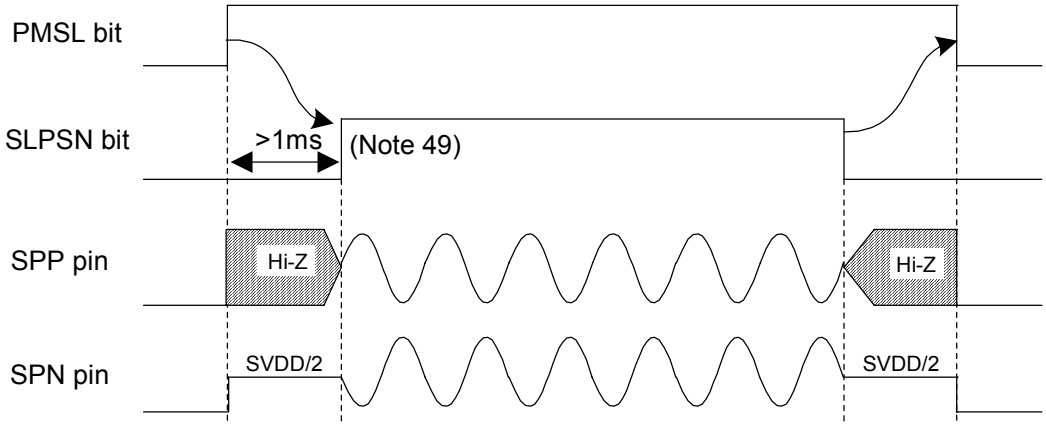
The speaker amplifier is powered-up/down by PMSL bit. When PMSL bit is "0", both SPP and SPN pins are pulled-down to VSS1 by 100kΩ (typ). When PMSL bit is "1" and SLPSN bit is "0", the speaker amplifier enters power-save mode. In this mode, the SPP pin is placed in Hi-Z state and the SPN pin outputs SVDD/2 voltage.

When the PMSL bit is "1" after the PDN pin is changed from "L" to "H", the SPP and SPN pins rise up in power-save mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to SVDD/2 voltage. Because the SPP and SPN pins rise up in power-save mode, pop noises are reduced. When the AK4954A is powered-down, a pop noise can also be reduced by first entering power-save mode.

*** When shut-down the AK4954A in low voltage mode (LSV bit = "1"), PMSL bit must be set to "0" before bringing the PDN pin to "L".**

PMSL bit	SLPSN bit	Mode	SPP pin	SPN pin	
0	x	Power-down	Pull-down to VSS1	Pull-down to VSS1	(default)
1	0	Power-save	Hi-Z	SVDD/2	
	1	Normal Operation	Normal Operation	Normal Operation	

Table 82 Speaker Amplifier Mode Setting (x: Don't care)



Note 49. This time needs 15ms or more in low voltage mode (LSV bit= "1").

Figure 49. Power-up/Power-down Timing for Speaker Amplifier

■ Thermal Shutdown Function

When the internal device temperature rises up irregularly (E.g. Output pins of speaker amplifier are shortened.), the charge pump, headphone amplifier or speaker amplifier is automatically powered down and then THDET bit becomes "1".

When the internal temperature goes down and the thermal shutdown is released, the charge pump, speaker amplifier or headphone amplifier is powered up automatically and THDET bit returns to "0".

■ Stereo Line Output (LOUT/ROUT pin, LOSEL bit = "1")

When LOSEL bit is set to "1", L and R channel signals of DAC are output in single-ended format via LOUT and ROUT pins. The stereo line output is valid at SVDD = 2.5~3.5V. The same voltage as AVDD must be supplied to the stereo lineout. It is not available in low voltage mode (LSV bit = "1").

When DACSL bit is "0", output signals are muted and LOUT and ROUT pins output common voltage. The load impedance is 10kΩ (min.). When the PMSL bit = "0" and SLPSN bit = "1", the stereo line output enters power-down mode and the output is pulled-down to VSS1 by 100kΩ(typ). When the SLPSN bit is "0", stereo line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMSL bit when SLPSN bit = "0". In this case, output signal line should be pulled-down by 20kΩ after AC coupled as Figure 51. Rise/Fall time is 300ms (max) when C=1μF and R_L=10kΩ. When PMSL bit = SLPSN bit = "1", stereo line output is in normal operation.

SLG1-0 bits set the gain of stereo line output.

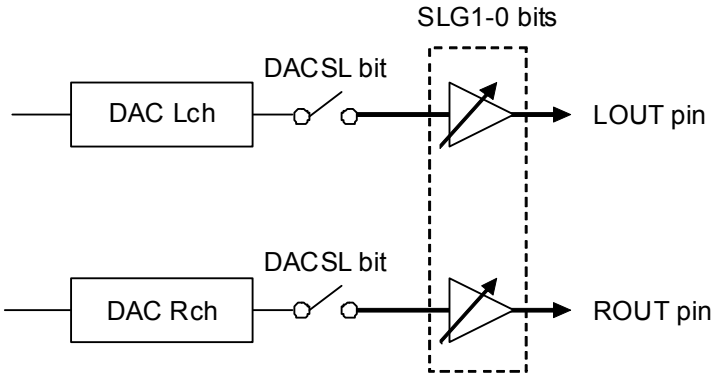


Figure 50. Stereo Line Output

PMSL bit	SLPSN bit	Mode	LOUT/ROUT pins	
0	0	Power-down	Fall down to VSS1	(default)
	1	Power-down	Pull-down to VSS1	
1	0	Power Save	Rise up to Common Voltage	
	1	Normal Operation	Normal Operation	

Table 83. Stereo Line Output Mode Select

SLG1-0 bits	Gain	
00	0dB	(default)
01	+2dB	
10	+4dB	
11	+6dB	

Table 84. Stereo Lineout Volume Setting (LOSEL bit = "1")

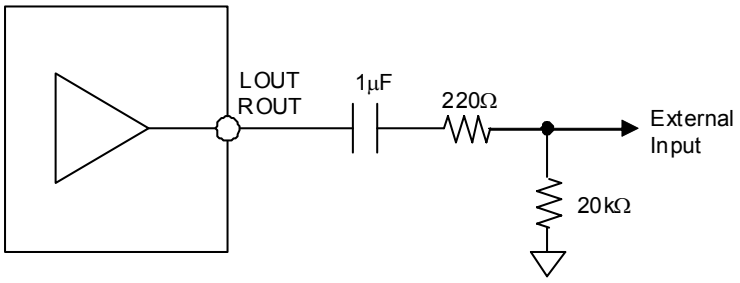


Figure 51. External Circuit for Stereo Line Output (in case of using a Pop Noise Reduction Circuit)

[Stereo Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)]

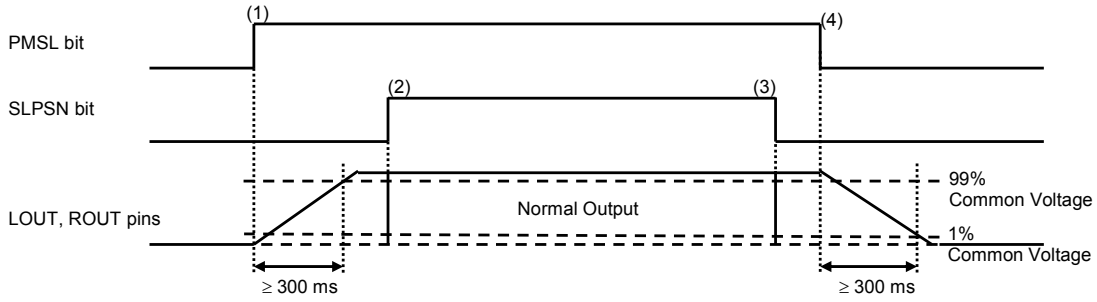


Figure 52. Stereo Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)

(1) Set PMSL bit = "1". Stereo line output exits power-down mode.
LOUT and ROUT pins rise up to common voltage. Rise time to 99% common voltage is 200ms (max. 300ms) when C=1μF.
(2) Set SLPSN bit = "1" after LOUT and ROUT pins rise up. Stereo line output exits power-save mode.
Stereo line output is enabled.
(3) Set SLPSN bit = "0". Stereo line output enters power-save mode.
(4) Set PMSL bit = "0". Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to 1% of the common voltage. Fall time is 200ms (max. 300ms) when C=1μF.

[Stereo Line Output Control Sequence (SLPSN bit = "1": in case of not using a Pop Noise Reduction Circuit)]

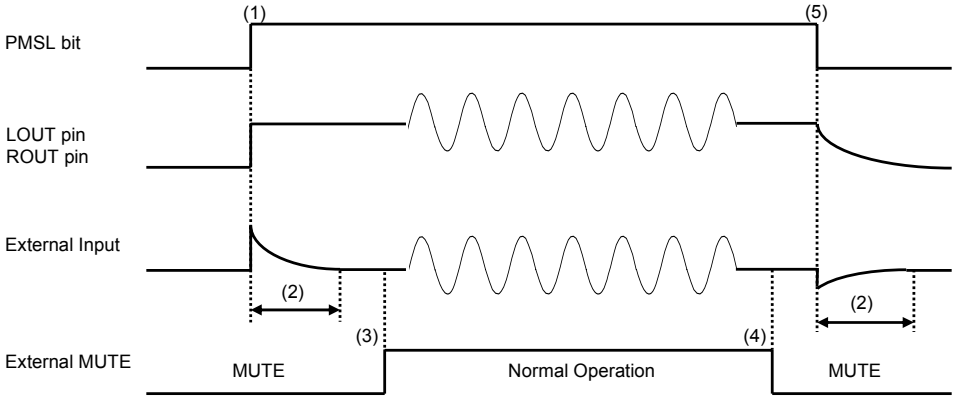


Figure 53. Stereo Line Output Control Sequence (SLPSN bit = "1": in case of not using a Pop Noise Reduction Circuit)

(1) Set PMSL bit = "1". Stereo line output is powered-up.
LOUT and ROUT pins rise up to common voltage.
(2) Time constant is defined according to external capacitor (C) and resistor (R_L).
(3) Release external MUTE when the external input is stabled.
Stereo line output is enabled.
(4) Set external MUTE ON
(5) Set PMSL bit = "0". Stereo line output is powered-down.
LOUT and ROUT pins fall down.

■ Serial Control Interface (I²C-bus)

The AK4954A supports the fast-mode I²C-bus (max: 400kHz). Pull-up resistors at the SDA and SCL pins must be connected to (TVDD+0.3)V or less voltage.

1. WRITE Operations

Figure 54 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 60). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010010". If the slave address matches that of the AK4954A, the AK4954A generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 61). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4954A. The format is MSB first 8bits (Figure 56). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 57). The AK4954A generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 60).

The AK4954A can perform more than one byte write operation per sequence. After receipt of the third byte the AK4954A generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 8FH prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 62) except for the START and STOP conditions.

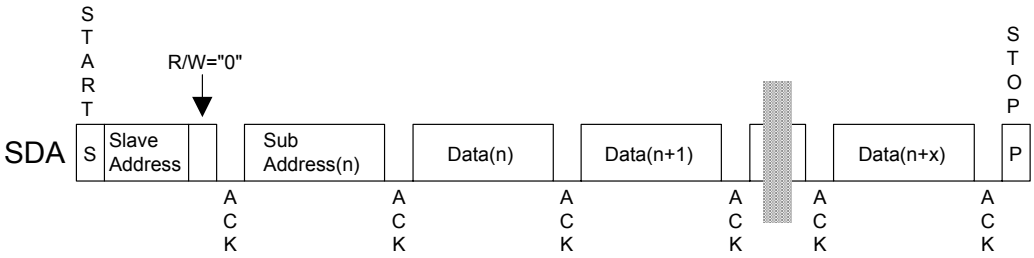


Figure 54. Data Transfer Sequence in I²C Bus Mode

0	0	1	0	0	1	0	R/W

Figure 55. The First Byte

A7	A6	A5	A4	A3	A2	A1	A0

Figure 56. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 57. The Third Byte

2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4954A. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 8FH prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK4954A supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-1. CURRENT ADDRESS READ

The AK4954A has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4954A generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4954A ceases the transmission.

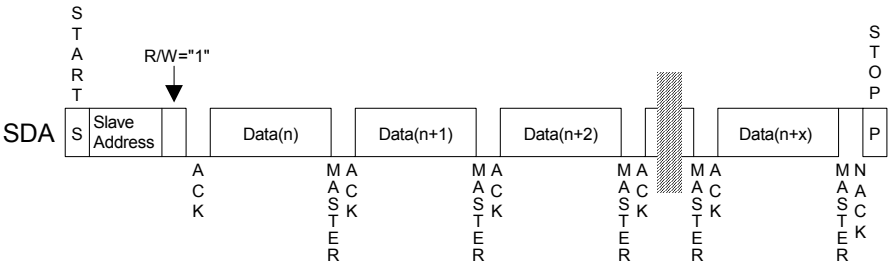


Figure 58. Current Address Read

2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4954A then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4954A ceases the transmission.

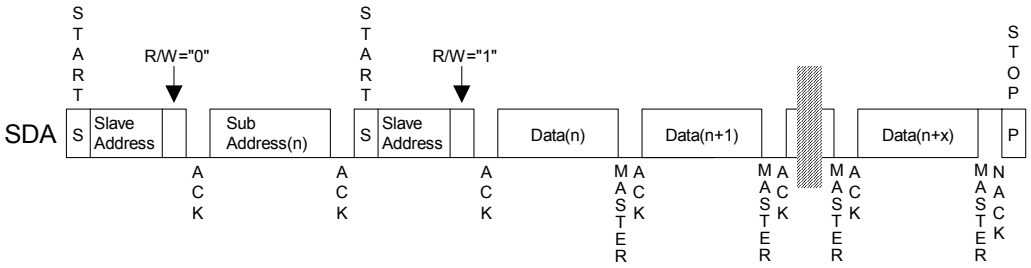


Figure 59. Random Address Read

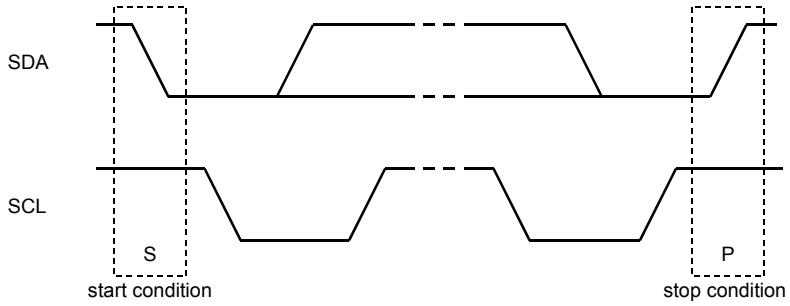


Figure 60. Start Condition and Stop Condition

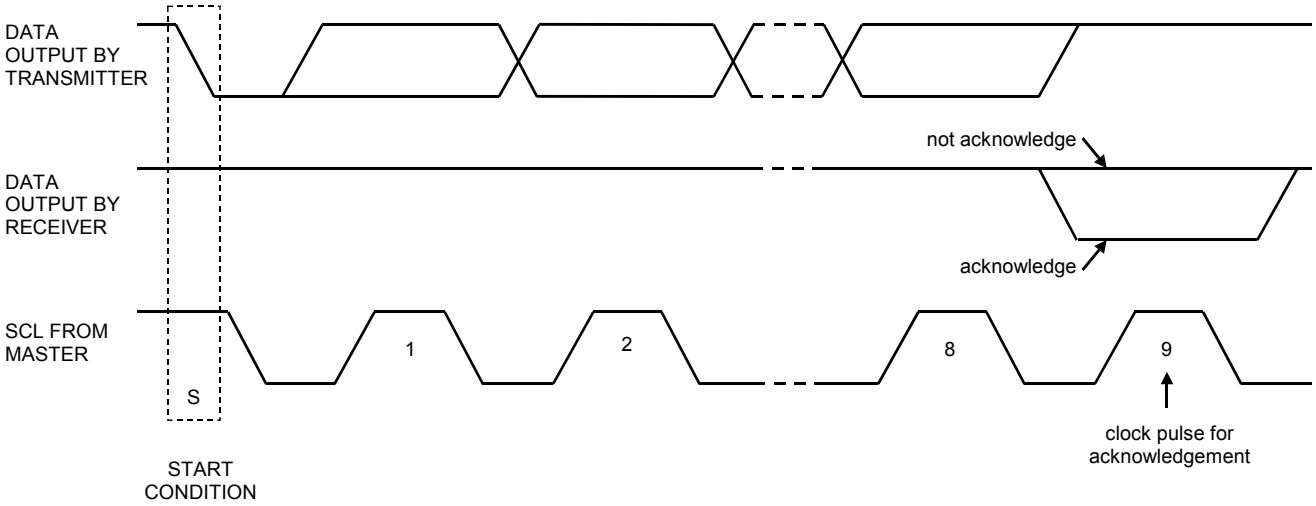


Figure 61. Acknowledge (I^2C Bus)

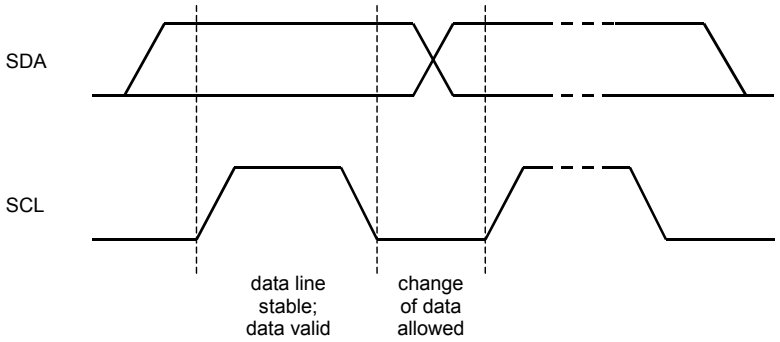


Figure 62. Bit Transfer (I^2C Bus)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	0	LSV	PMDAC	PMADR	PMADL
01H	Power Management 2	0	0	PMHPR	PMHPL	M/S	PMPLL	PMSL	LOSEL
02H	Signal Select 1	SLPSN	0	DACSL	MPSEL	PMMP	MGAIN2	MGAIN1	MGAIN0
03H	Signal Select 2	SLG1	SLG0	0	0	INL1	INL0	INR1	INR0
04H	Signal Select 3	0	0	1	1	PTS1	PTS0	MOFF	MONO
05H	Mode Control 1	0	PLL2	PLL1	PLL0	BCKO	DIF2	DIF1	DIF0
06H	Mode Control 2	CM1	CM0	0	0	FS3	FS2	FS1	FS0
07H	Mode Control 3	OVFL	THDET	SMUTE	DVOLC	0	IVOLC	LPMIC	LPDA
08H	Digital MIC	0	TEST	PMDMR	PMDML	DCLKE	0	DCLKP	DMIC
09H	Timer Select	ADRST1	ADRST 0	1	1	OVTM1	OVTM0	DVTM1	DVTM0
0AH	ALC Timer Select	IVTM1	IVTM0	0	0	WTM1	WTM0	RFST1	RFST0
0BH	ALC Mode Control 1	ALCEQN	0	ALC	RGAIN2	RGAIN1	RGAIN0	LMTH1	LMTH0
0CH	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
0DH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
0EH	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
0FH	Reserved	0	0	0	0	0	0	0	0
10H	Reserved	0	0	0	0	0	0	0	0
11H	Reserved	0	0	0	0	0	0	0	0
12H	HP Output Control	HPZ	0	0	0	0	0	0	0
13H	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
14H	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
15H	BEEP Frequency	BPCNT	0	0	0	0	0	BPFR1	BPFR0
16H	BEEP ON Time	BPON7	BPON6	BPON5	BPON4	BPON3	BPON2	BPON1	BPON0
17H	BEEP OFF Time	BPOFF7	BPOFF6	BPOFF5	BPOFF4	BPOFF3	BPOFF2	BPOFF1	BPOFF0
18H	BEEP Repeat Count	0	BPTM6	BPTM5	BPTM4	BPTM3	BPTM2	BPTM1	BPTM0
19H	BEEP Volume Control	BPOUT	0	0	BPLVL4	BPLVL3	BPLVL2	BPLVL1	BPLVL0
1AH	Reserved	0	0	0	0	0	0	0	0
1BH	Digital Filter Select 1	0	0	0	0	SDAD	HPFC1	HPFC0	HPFAD
1CH	Digital Filter Select 2	GN1	GN0	EQ0	FIL3	0	0	LPF	HPF
1DH	Digital Filter Mode	PMDRC	0	0	0	0	PFDAC	ADCPF	PFSDO
1EH	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1FH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
20H	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
21H	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
22H	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
23H	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
24H	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
25H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
26H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
27H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
28H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
29H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
2AH	EQ Co-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
2BH	EQ Co-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
2CH	EQ Co-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
2DH	EQ Co-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
2EH	EQ Co-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
2FH	EQ Co-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 3	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Reserved	0	0	0	0	0	0	0	0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
50H	DRC Mode Control	0	DLMAT2	DLMAT1	DLMAT0	DRGAIN1	DRGAIN0	DRCC1	DRCC0
51H	NS Control	0	0	DRCM1	DRCM0	0	NSLPF	NSHPF	NSCE
52H	NS Gain & ATT Control	0	NSGAIN2	NSGAIN1	NSGAIN0	0	NSATT2	NSATT1	NSATT0
53H	NS On Level	NSIAF1	NSIAF0	0	NSTHL4	NSTHL3	NSTHL2	NSTHL1	NSTHL0
54H	NS Off Level	NSOAF1	NSOAF0	0	NSTHH4	NSTHH3	NSTHH2	NSTHH1	NSTHH0
55H	NS Reference Select	0	0	0	0	NSREF3	NSREF2	NSREF1	NSREF0
56H	NS LPF Co-efficient 0	NSLA7	NSLA6	NSLA5	NSLA4	NSLA3	NSLA2	NSLA1	NSLA0
57H	NS LPF Co-efficient 1	0	0	NSLA13	NSLA12	NSLA11	NSLA10	NSLA9	NSLA8
58H	NS LPF Co-efficient 2	NSLB7	NSLB6	NSLB5	NSLB4	NSLB3	NSLB2	NSLB1	NSLB0
59H	NS LPF Co-efficient 3	0	0	NSLB13	NSLB12	NSLB11	NSLB10	NSLB9	NSLB8
5AH	NS HPF Co-efficient 0	NSHA7	NSHA6	NSHA5	NSHA4	NSHA3	NSHA2	NSHA1	NSHA0
5BH	NS HPF Co-efficient 1	0	0	NSHA13	NSHA12	NSHA11	NSHA10	NSHA9	NSHA8
5CH	NS HPF Co-efficient 2	NSHB7	NSHB6	NSHB5	NSHB4	NSHB3	NSHB2	NSHB1	NSHB0
5DH	NS HPF Co-efficient 3	0	0	NSHB13	NSHB12	NSHB11	NSHB10	NSHB9	NSHB8
5EH	Reserved	0	0	0	0	0	0	0	0
5FH	Reserved	0	0	0	0	0	0	0	0
60H	DVLC Filter Select	DLLPF1	DLLPF0	DMHPF1	DMHPF0	DMLPF1	DMLPF0	DHHPF1	DHHPF0
61H	DVLC Mode Control	DVRGAIN2	DVRGAIN1	DVRGAIN0	DVLMAT2	DVLMAT1	DVLMAT0	DAF1	DAF0
62H	DVLCL Curve X1	0	0	VL1X5	VL1X4	VL1X3	VL1X2	VL1X1	VL1X0
63H	DVLCL Curve Y1	0	0	VL1Y5	VL1Y4	VL1Y3	VL1Y2	VL1Y1	VL1Y0
64H	DVLCL Curve X2	0	0	VL2X5	VL2X4	VL2X3	VL2X2	VL2X1	VL2X0
65H	DVLCL Curve Y2	0	0	VL2Y5	VL2Y4	VL2Y3	VL2Y2	VL2Y1	VL2Y0
66H	DVLCL Curve X3	0	0	0	VL3X4	VL3X3	VL3X2	VL3X1	VL3X0
67H	DVLCL Curve Y3	0	0	0	VL3Y4	VL3Y3	VL3Y2	VL3Y1	VL3Y0
68H	DVLCL Slope 1	0	L1G6	L1G5	L1G4	L1G3	L1G2	L1G1	L1G0
69H	DVLCL Slope 2	0	L2G6	L2G5	L2G4	L2G3	L2G2	L2G1	L2G0
6AH	DVLCL Slope 3	0	L3G6	L3G5	L3G4	L3G3	L3G2	L3G1	L3G0
6BH	DVLCL Slope 4	0	L4G6	L4G5	L4G4	L4G3	L4G2	L4G1	L4G0
6CH	DVLCM Curve X1	0	0	VM1X5	VM1X4	VM1X3	VM1X2	VM1X1	VM1X0
6DH	DVLCM Curve Y1	0	0	VM1Y5	VM1Y4	VM1Y3	VM1Y2	VM1Y1	VM1Y0
6EH	DVLCM Curve X2	0	0	VM2X5	VM2X4	VM2X3	VM2X2	VM2X1	VM2X0
6FH	DVLCM Curve Y2	0	0	VM2Y5	VM2Y4	VM2Y3	VM2Y2	VM2Y1	VM2Y0
70H	DVLCM Curve X3	0	0	0	VM3X4	VM3X3	VM3X2	VM3X1	VM3X0
71H	DVLCM Curve Y3	0	0	0	VM3Y4	VM3Y3	VM3Y2	VM3Y1	VM3Y0
72H	DVLCM Slope 1	0	M1G6	M1G5	M1G4	M1G3	M1G2	M1G1	M1G0
73H	DVLCM Slope 2	0	M2G6	M2G5	M2G4	M2G3	M2G2	M2G1	M2G0
74H	DVLCM Slope 3	0	M3G6	M3G5	M3G4	M3G3	M3G2	M3G1	M3G0
75H	DVLCM Slope 4	0	M4G6	M4G5	M4G4	M4G3	M4G2	M4G1	M4G0
76H	DVLCH Curve X1	0	0	VH1X5	VH1X4	VH1X3	VH1X2	VH1X1	VH1X0
77H	DVLCH Curve Y1	0	0	VH1Y5	VH1Y4	VH1Y3	VH1Y2	VH1Y1	VH1Y0
78H	DVLCH Curve X2	0	0	VH2X5	VH2X4	VH2X3	VH2X2	VH2X1	VH2X0
79H	DVLCH Curve Y2	0	0	VH2Y5	VH2Y4	VH2Y3	VH2Y2	VH2Y1	VH2Y0
7AH	DVLCH Curve X3	0	0	0	VH3X4	VH3X3	VH3X2	VH3X1	VH3X0
7BH	DVLCH Curve Y3	0	0	0	VH3Y4	VH3Y3	VH3Y2	VH3Y1	VH3Y0
7CH	DVLCH Slope 1	0	H1G6	H1G5	H1G4	H1G3	H1G2	H1G1	H1G0
7DH	DVLCH Slope 2	0	H2G6	H2G5	H2G4	H2G3	H2G2	H2G1	H2G0
7EH	DVLCH Slope 3	0	H3G6	H3G5	H3G4	H3G3	H3G2	H3G1	H3G0
7FH	DVLCH Slope 4	0	H4G6	H4G5	H4G4	H4G3	H4G2	H4G1	H4G0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
80H	DVLCL LPF Co-efficient 0	DLLA7	DLLA6	DLLA5	DLLA4	DLLA3	DLLA2	DLLA1	DLLA0
81H	DVLCL LPF Co-efficient 1	0	0	DLLA13	DLLA12	DLLA11	DLLA10	DLLA9	DLLA8
82H	DVLCL LPF Co-efficient 2	DLLB7	DLLB6	DLLB5	DLLB4	DLLB3	DLLB2	DLLB1	DLLB0
83H	DVLCL LPF Co-efficient 3	0	0	DLLB13	DLLB12	DLLB11	DLLB10	DLLB9	DLLB8
84H	DVLCM HPF Co-efficient 0	DMHA7	DMHA6	DMHA5	DMHA4	DMHA3	DMHA2	DMHA1	DMHA0
85H	DVLCM HPF Co-efficient 1	0	0	DMHA13	DMHA12	DMHA11	DMHA10	DMHA9	DMHA8
86H	DVLCM HPF Co-efficient 2	DMHB7	DMHB6	DMHB5	DMHB4	DMHB3	DMHB2	DMHB1	DMHB0
87H	DVLCM HPF Co-efficient 3	0	0	DMHB13	DMHB12	DMHB11	DMHB10	DMHB9	DMHB8
88H	DVLCM LPF Co-efficient 0	DMLA7	DMLA6	DMLA5	DMLA4	DMLA3	DMLA2	DMLA1	DMLA0
89H	DVLCM LPF Co-efficient 1	0	0	DMLA13	DMLA12	DMLA11	DMLA10	DMLA9	DMLA8
8AH	DVLCM LPF Co-efficient 2	DMLB7	DMLB6	DMLB5	DMLB4	DMLB3	DMLB2	DMLB1	DMLB0
8BH	DVLCM LPF Co-efficient 3	0	0	DMLB13	DMLB12	DMLB11	DMLB10	DMLB9	DMLB8
8CH	DVLCH HPF Co-efficient 0	DHHA7	DHHA6	DHHA5	DHHA4	DHHA3	DHHA2	DHHA1	DHHA0
8DH	DVLCH HPF Co-efficient 1	0	0	DHHA13	DHHA12	DHHA11	DHHA10	DHHA9	DHHA8
8EH	DVLCH HPF Co-efficient 2	DHHB7	DHHB6	DHHB5	DHHB4	DHHB3	DHHB2	DHHB1	DHHB0
8FH	DVLCH HPF Co-efficient 3	0	0	DHHB13	DHHB12	DHHB11	DHHB10	DHHB9	DHHB8

Note 50. PDN pin = “L” resets the registers to their default values.
Note 51. The bits defined as 0 must contain a “0” value. The bits defined as 1 must contain a “1” value.
Note 52. Writing access to 90H ~ FFH is prohibited.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	0	LSV	PMDAC	PMADR	PMADL
R/W		R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMADL: Microphone Amplifier Lch and ADC Lch Power Management
0: Power-down (default)
1: Power-up
When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (2115/fs=48ms @44.1kHz, ADRST1-0 bits = "00") starts. After initializing, digital data of the ADC is output.

PMADR: Microphone Amplifier Rch and ADC Rch Power Management
0: Power-down (default)
1: Power-up
When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (2115/fs=48ms @44.1kHz, ADRST1-0 bits = "00") starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Power Management
0: Power-down (default)
1: Power-up

LSV: Low Voltage Operation Mode of the Speaker Amplifier
0: Normal mode: SVDD=1.8V ~ 5.5V (default)
1: Low voltage mode: SVDD=0.9V ~ 2.0V

PMBP: BEEP Generating Circuit Power Management
0: Power-down (default)
1: Power-up

PMVCM: VCOM Power Management
0: Power-down (default)
1: Power-up

PMPFIL: Programmable Filter Block Power Management
0: Power-down (default)
1: Power-up

All blocks can be powered-down by writing "0" to the address "00H", PMPLL, PMMP, PMHPL, PMHPR, PMSL, PMDML, PMDMR and PMDRC bits. In this case, register values are maintained.

PMVCM bit must be "1" when one of bocks is powered-up. PMVCM bit can only be "0" when the address "00H" and all power management bits (PMPLL, PMMP, PMHPL, PMHPR, PMSL, PMDML, PMDMR and PMDRC) are "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	0	PMHPR	PMHPL	M/S	PMPLL	PMSL	LOSEL
R/W		R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LOSEL: Stereo Line Output Select
0: Speaker Output (SPP/SPN pins) (default)
1: Stereo Line Output (LOUT/ROUT pins)

PMSL: Speaker Amplifier or Stereo Line Output Power Management.
0: Power-down (default)
1: Power-up

PMPLL: PLL Power Management
0: EXT Mode and Power-down (default)
1: PLL Mode and Power-up

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

PMHPL: Lch Headphone Amplifier and Charge Pump Power Management
0: Power-down (default)
1: Power-up

PMHPR: Rch Headphone Amplifier and Charge Pump Power Management
0: Power-down (default)
1: Power-up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select 1	SLPSN	0	DACSL	MPSEL	PMMP	MGAIN2	MGAIN1	MGAIN0
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

MGAIN2-0: Microphone Amplifier Gain Control (Table 22)
Default: "010" (+20dB)

PMMP: MPWR pin Power Management
0: Power-down: Hi-Z (default)
1: Power-up

MPSEL: MPWR Output Select
0: MPWR1 pin (default)
1: MPWR2 pin

DACS: Signal Switch Control from DAC to Speaker Amplifier or Stereo Line Amplifier
0: OFF (default)
1: ON
When DACS bit is "1", DAC output signal is input to Speaker Amplifier or Stereo Line Amplifier.

SLPSN: Speaker Amplifier or Stereo Line Amplifier Power-Save Mode
LOSEL bit = "0" (Speaker Output Select)
0: Power-Save Mode (default)
1: Normal Operation
When SLPSN bit is "0", Speaker Amplifier is in power-save mode. In this mode, the SPP pin goes to Hi-Z and the SPN pin outputs SVDD/2 voltage. When PMSL bit = "1", SLPSN bit is enabled. After the PDN pin is set to "L", Speaker Amplifier is in power-down mode since PMSL bit is "0".

LOSEL bit = "1" (Stereo Line Output Select)
0: Power-Save Mode (default)
1: Normal Operation
When SLPSN bit is "0", Stereo line output is in power-save mode. In this mode, the LOUT/ROUT pins outputs SVDD/2 voltage. When PMSL bit = "1", SLPSN bit is enabled. After the PDN pin is set to "L", Stereo line output is in power-down mode since PMSL bit is "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	SLG1	SLG0	0	0	INL1	INL0	INR1	INR0
R/W		R/W	R/W	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

INR1-0: ADC Rch Input Source Select (Table 21)
Default: 00 (RIN1 pin)

INL1-0: ADC Lch Input Source Select (Table 21)
Default: 00 (LIN1 pin)

SLG1-0: Speaker Amplifier and Stereo Line Amplifier Output Gain Select (Table 80, Table 84)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Signal Select 3	0	0	1	1	PTS1	PTS0	MOFF	MONO
R/W		R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	0	1	0	0

MONO: Monaural mixing setting of the DAC output
0: Stereo (default)
1: Mono Mix
When MONO bit = "1", both L and R channels DAC output signals are (L+R)/2.

MOFF: Soft Transition Control of "BEEP → Headphone" Connection ON/OFF
0: Enable (default)
1: Disable

PTS1-0: Soft Transition Time of "BEEP → Headphone" Connection ON/OFF
Default: "01" (Table 72)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 1	0	PLL2	PLL1	PLL0	BCKO	DIF2	DIF1	DIF0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	1	0

DIF2-0: Audio Interface Format (Table 18)
Default: "010" (24-bit MSB justified)

BCKO: BICK Output Frequency Setting in Master Mode (Table 9)

PLL2-0: PLL Reference Clock Select (Table 5)
Default: "010" (MCKI, 11.2896MHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Mode Control 2	CM1	CM0	0	0	FS3	FS2	FS1	FS0
R/W		R/W	R/W	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	1

FS3-0: Sampling frequency Setting (Table 6, Table 11, Table 14)
Default: "1001" (fs=44.1kHz)

CM1-0: MCKI Input Frequency Setting in EXT mode. (Table 10, Table 13)
Default: "00" (256fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Mode Control 3	OVFL	THDET	SMUTE	DVOLC	0	IVOLC	LPMIC	LPDA
R/W		R/W	R	R/W	R/W	R	R/W	R/W	R/W
Default		0	0	0	1	0	1	0	0

LPDA: Low-Power Consumption Mode of DAC + HP (Table 79)
0: Normal Operation (default)
1: Low-power consumption mode

LPMIC: Low-Power Consumption Mode of Microphone Amplifier (Table 23)
0: Normal Operation (default)
1: Low-power consumption mode

IVOLC: Input Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume levels, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = "0", IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively. PMPFIL bit must be "0" when changing the IVOLC bit setting.

DVOLC: Output Digital Volume 2 Control Mode Select
0: Independent
1: Dependent (default)
When DVOLC bit = "1", DVL7-0 bits control both Lch and Rch volume levels, while register values of DVL7-0 bits are not written to DVR7-0 bits. When DVOLC bit = "0", DVL7-0 bits control Lch level and DVR7-0 bits control Rch level, respectively.

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted

THDET: Thermal Shutdown Detection Result
0: Normal Operation (default)
1: During Thermal Shutdown

OVFL: ADC Overflow Output Enable (OVF pin)
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Digital Microphone	0	TEST	PMDMR	PMDML	DCLKE	0	DCLKP	DMIC
R/W		R	R/W	R/W	R/W	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

DMIC: Digital Microphone Connection Select
0: Analog Microphone (default)
1: Digital Microphone

DCLKP: Data Latching Edge Select
0: Lch data is latched on the DMCLK rising edge (“↑”). (default)
1: Lch data is latched on the DMCLK falling edge (“↓”).

DCLKE: DMCLK pin Output Clock Control
0: “L” Output (default)
1: 64fs Output

PMDML/R: Input Signal Select with Digital Microphone (Table 20)
Default: “00”
ADC digital block is powered-down by PMDML = PMDMR bits = “0” when selecting a digital microphone input (DMIC bit = “1”, INL/R bits = “00”, “01” or “10”).

TEST: Device TEST mode Enable.
0: Normal operation (default)
1: TEST mode
TEST bit must be always “0”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Timer Select	ADRST1	ADRST0	1	1	OVTM1	OVTM0	DVTM1	DVTM0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	1	0	1	0

DVTM1-0: Output Digital Volume Soft Transition Time Setting (Table 70)
Default: “10” (576/fs)
This is the transition time between DVL/R7-0 bits = 00H and 90H.

OVTM1-0: ADC Overflow Output Hold Time Setting (Table 27)
Default: “10” (128/fs)

ADRST1-0: ADC Initialization Cycle Setting (Table 17)
00: 2115/fs (default)
01: 4227/fs
10: 267/fs
11: 1059/fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ALC Timer Select	IVTM1	IVTM0	0	0	WTM1	WTM0	RFST1	RFST0
R/W		R/W	R/W	R	R	R/W	R/W	R/W	R/W
Default		0	1	0	0	0	0	0	0

RFST1-0: ALC First recovery Speed (Table 37)
Default: "00" (0.0032dB)

WTM1-0: ALC Recovery Waiting Period (Table 34)
Default: "00" (128/fs)
A period of recovery operation when any limiter operation does not occur during ALC operation

IVTM1-0: Input Digital Volume Soft Transition Time Setting (Table 41)
Default: "01" (944/fs)
A transition time when changing IVL7-0/IVR7-0 bits to F1H from 05H.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 1	ALCEQN	0	ALC	RGAIN2	RGAIN1	RGAIN0	LMTH1	LMTH0
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 32)
Default: "00"

RGAIN2-0: ALC Recovery Gain Step (Table 35)
Default: "000" (0.00424dB)

ALC: ALC Enable
0: ALC Disable (default)
1: ALC Enable

ALCEQN: ALC EQ Enable
0: ALC EQ On (default)
1: ALC EQ Off

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	ALC Mode Control 2	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

REF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (Table 36)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
0EH	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IVOL7-0, IVOR7-0: Digital Input Volume; 0.375dB step, 242 Level. (Table 40)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	HP Output Control	HPZ	0	0	0	0	0	0	0
R/W		R/W	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

HPZ: Pull-down Setting of HP Amplifier
0: Pull-down by a 10Ω(typ) resistor. (default)
1: Hi-Z
When using HPZ bit, set HPZ bit to "1" before starting a speaker amplifier operation, and then write registers according to the sequence in "■ Speaker Amplifier Output". Set HPZ bit to "0" before starting a headphone amplifier operation, and then write registers according to the sequence in "■ Headphone Amplifier Output".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
14H	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

DVL7-0, DVR7-0: Digital Output Volume (Table 69)
Default: "0CH" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	BEEP Frequency	BPCNT	0	0	0	0	0	BPFR1	BPFR0
R/W		R/W	R	R	R	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPFR1-0: BEEP Signal Output Frequency Setting (Table 73)
Default: "00H"

BPCNT: BEEP Signal Output Mode Setting
0: Single Output Mode. (default)
1: Continuous Mode
In single output mode, the BEEP signal is output by the repeat times set by BPTM6-0 bits.
In continuous mode, the BEEP signal is output while BPCNT bit is "1".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	BEEP ON Time	BPON7	BPON6	BPON5	BPON4	BPON3	BPON2	BPON1	BPON0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPON7-0: BEEP Output ON-time Setting (Table 74)
Default: "00H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
17H	BEEP OFF Time	BPOFF7	BPOFF6	BPOFF5	BPOFF4	BPOFF3	BPOFF2	BPOFF1	BPOFF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPOFF7-0: BEEP Output OFF-time Setting (Table 75)
Default: "00H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	BEEP Repeat Count	0	BPTM6	BPTM5	BPTM4	BPTM3	BPTM2	BPTM1	BPTM0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPTM6-0: BEEP Output Repeat Count Setting (Table 76)
Default: "00H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
19H	BEEP Volume Control	BPOUT	0	0	BPLVL4	BPLVL3	BPLVL2	BPLVL1	BPLVL0
R/W		R/W	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPLVL4-0: BEEP Output level Setting (Table 77)
Default: "0H" (0dB)

BPOUT: BEEP Signal Control
0: OFF (default)
1: ON
When BPCNT bit = "0", the beep signal starts outputting by setting BPOUT bit = "1". The Beep signal stops after the number of times that is set by BPTM6-0 bit, and BPOUT bit is set to "0" automatically.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1BH	Digital Filter Select 1	0	0	0	0	SDAD	HPFC1	HPFC0	HPFAD
R/W		R	R	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

HPFAD: HPF1 Control after ADC
0: OFF
1: ON (default)
When HPFAD bit is “1”, the settings of HPFC1-0 bits are enabled. When HPFAD bit is “0”, the audio data passes the HPFAD block by 0dB gain.
When PMADL bit = “1” or PMADR bit = “1”, set HPFAD bit to “1”.

HPFC1-0: Cut-off Frequency Setting of HPF1 (ADC) (Table 29)
Default: “00” (3.4Hz @ fs = 44.1kHz)

SDAD: ADC Digital Filter Select
0: Sharp Roll-Off Filter (default)
1: Short Delay Sharp Roll-Off Filter

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	Digital Filter Select 2	GN1	GN0	EQ0	FIL3	0	0	LPF	HPF
R/W		R/W	R/W	R/W	R/W	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

HPF: HPF2 Coefficient Setting Enable
0: OFF (default)
1: ON
When HPF bit is “1”, the settings of F1A13-0 and F1B13-0 bits are enabled. When HPF bit is “0”, the audio data passes the HPF2 block by is 0dB gain.

LPF: LPF Coefficient Setting Enable
0: OFF (default)
1: ON
When LPF bit is “1”, the settings of F2A13-0 and F2B13-0 bits are enabled. When LPF bit is “0”, the audio data passes the LPF block by 0dB gain.

FIL3: FIL3 (Stereo Emphasis Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When FIL3 bit = “1”, the settings of F3A13-0 and F3B13-0 bits are enabled. When FIL3 bit = “0”, FIL3 block is OFF (MUTE).

EQ0: EQ0 (Gain Compensation Filter) Coefficient Setting Enable
0: OFF (default)
1: ON
When EQ0 bit = “1”, the settings of E0A15-0, E0B13-0 and E0C15-0 bits are enabled. When EQ0 bit = “0”, the audio data passes the EQ0 block by 0dB gain.

GN1-0: Gain Setting of the Gain Block (Table 30)
Default: “00” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1DH	Digital Filter Mode	PMDRC	0	0	0	0	PFDAC	ADCPF	PFSDO
R/W		R/W	R	R	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

PFSDO: SDTO Output Signal Select
0: ADC (+ 1st order HPF) Output
1: Programmable Filter / ALC Output (default)

ADCPF: Programmable Filter / ALC Input Signal Select
0: SDTI
1: ADC Output (default)

PFDAC: DAC Input Signal Select
0: SDTI (default)
1: Programmable Filter / ALC Output

PMDRC: Dynamic Range Control Circuit Power Management
0: Power-down (default)
1: Power-up
When PMDRC bit = "1", register settings of address 50H~8FH are valid. When PMDRC bit = "0", the audio data passes the DRC block by 0dB gain.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1EH	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1FH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
20H	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
21H	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		F1A13-0 bits = 0x1FA9, F1B13-0 bits = 0x20AD							

F1A13-0, F1B13-0: HPF2 Coefficient (14bit x 2)
Default: F1A13-0 bits = 0x1FA9, F1B13-0 bits = 0x20AD
fc = 150Hz@fs=44.1kHz

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
22H	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
23H	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
24H	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
25H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

F2A13-0, F2B13-0: LPF Coefficient (14bit x 2)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
26H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
27H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
28H	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
29H	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
2AH	EQ Co-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
2BH	EQ Co-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
2CH	EQ Co-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
2DH	EQ Co-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
2EH	EQ Co-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
2FH	EQ Co-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

F3A13-0, F3B13-0: FIL3 (Stereo Emphasis Filter) Coefficient (14bit x 2)
Default: “0000H”

F3AS: FIL3 (Stereo Emphasis Filter) Select
0: HPF (default)
1: LPF

E0A15-0, E0B13-0, E0C15-C0: EQ0 (Gain Compensation Filter) Coefficient (14bit x 1 + 16bit x 2)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 3	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ1 bit is "1", the settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit is "0", the audio data passes the EQ1 block by 0dB gain.

EQ2: Equalizer 2 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ2 bit is "1", the settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit is "0", the audio data passes the EQ2 block by 0dB gain.

EQ3: Equalizer 3 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ3 bit is "1", the settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit is "0", the audio data passes the EQ3 block by 0dB gain.

EQ4: Equalizer 4 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ4 bit is "1", the settings of E4A15-0, E4B15-0 and E4C15-0 bits are enabled. When EQ4 bit is "0", the audio data passes the EQ4 block by 0dB gain.

EQ5: Equalizer 5 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ5 bit is "1", the settings of E5A15-0, E5B15-0 and E5C15-0 bits are enabled. When EQ5 bit is "0", the audio data passes the EQ5 block by 0dB gain.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: “0000H”

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: “0000H”

E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: “0000H”

E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
Default: “0000H”

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
50H	DRC Mode Control	0	DLMAT2	DLMAT1	DLMAT0	DRGAIN1	DRGAIN0	DRCC1	DRCC0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DRCC1-0: DRC Setting Enable (Table 66)
- 00: Disable (default)
- 01: Low
- 10: Middle
- 11: High

When DRCC1-0 bits are "00", the audio data passes the DRC block by 0dB gain.

DRGAIN1-0: DRC Recovery Speed Setting (Table 68)
Default: "00"

DLMAT2-0: DRC Attenuation Speed Setting (Table 67)
Default: "000"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
51H	NS Control	0	0	DRCM1	DRCM0	0	NSLPF	NSHPF	NSCE
R/W		R	R	R/W	R/W	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

NSCE: Noise Suppression Setting Enable
- 0: Disable (default)
- 1: Enable

When NSCE bit is "0", the audio data passes the Noise Suppression block by 0dB gain.

NSHPF: HPF for Noise Suppression Coefficient Setting Enable
- 0: Disable (default)
- 1: Enable

When NSHPF bit = "1", the settings of NSHA13-0 and NSHB13-0 bits are enabled. When NSHPF bit is "0", the audio data passes the HPF block by 0dB gain.

NSLPF: Noise Suppression LPF Coefficient Setting Enable
- 0: Disable (default)
- 1: Enable

When NSLPF bit = "1", the settings of NSLA13-0 and NSLB13-0 bits are enabled. When NSLPF bit is "0", the audio data passes the LPF block by 0dB gain.

DRCM1-0: DRC Input Signal Setting (Table 42)
Default: "00" (L = Lch, R = Rch)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
52H	NS Gain & ATT Control	0	NSGAIN2	NSGAIN1	NSGAIN0	0	NSATT2	NSATT1	NSATT0
R/W		R	R/W	R/W	R/W	R	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	1

NSATT2-0: Noise Suppression Attenuation Speed Setting (Table 46)
Default: "001"

NSGAIN2-0: Noise Suppression Recovery Speed Setting (Table 49)
Default: "001"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
53H	NS On Level	NSIAF1	NSIAF0	0	NSTHL4	NSTHL3	NSTHL2	NSTHL1	NSTHL0
	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
	Default	1	0	0	0	0	0	0	0

NSTHL4-0: Noise Suppression Threshold Low Level Setting (Table 44)
Default: "00H" (-36dB)

NSIAF1-0: Moving Avarage Parameter Setting at Noise Suppression Off (Table 43)
Default: "10" (1024/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
54H	NS Off Level	NSOAF1	NSOAF0	0	NSTHH4	NSTHH3	NSTHH2	NSTHH1	NSTHH0
	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
	Default	1	0	0	0	0	0	0	0

NSTHH4-0: Noise Suppression Threshold High Level Setting (Table 48)
Default: "00H" (-36dB)

NSOAF1-0: Moving Avarage Parameter Setting at Noise Suppression On (Table 47)
Default: "10" (16/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
55H	NS Reference Select	0	0	0	0	NSREF3	NSREF2	NSREF1	NSREF0
	R/W	R	R	R	R	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

NSREF3-0: Reference Value at Noise Suppression (Table 45)
Default: "0H" (-9dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
56H	NS LPF Co-efficient 0	NSLA7	NSLA6	NSLA5	NSLA4	NSLA3	NSLA2	NSLA1	NSLA0
57H	NS LPF Co-efficient 1	0	0	NSLA13	NSLA12	NSLA11	NSLA10	NSLA9	NSLA8
58H	NS LPF Co-efficient 2	NSLB7	NSLB6	NSLB5	NSLB4	NSLB3	NSLB2	NSLB1	NSLB0
59H	NS LPF Co-efficient 3	0	0	NSLB13	NSLB12	NSLB11	NSLB10	NSLB9	NSLB8
5AH	NS HPF Co-efficient 0	NSHA7	NSHA6	NSHA5	NSHA4	NSHA3	NSHA2	NSHA1	NSHA0
5BH	NS HPF Co-efficient 1	0	0	NSHA13	NSHA12	NSHA11	NSHA10	NSHA9	NSHA8
5CH	NS HPF Co-efficient 2	NSHB7	NSHB6	NSHB5	NSHB4	NSHB3	NSHB2	NSHB1	NSHB0
5DH	NS HPF Co-efficient 3	0	0	NSHB13	NSHB12	NSHB11	NSHB10	NSHB9	NSHB8
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

NSLA13-0, NSLB13-0: Noise Suppression LPF Coefficient (14bit x 2)
Default: "0000H"

NSHA13-0, NSHB13-0: Noise Suppression HPF Coefficient (14bit x 2)
Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
60H	DVLC Filter Select	DLLPF1	DLLPF0	DMHPF1	DMHPF0	DMLPF1	DMLPF0	DHHPF1	DHHPF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DHHPF1-0: DVLC High Frequency Range HPF Setting (Table 59)
00: Disable (default)
01: 1st order HPF
10: 2nd order HPF
11: N/A
When DHHPF1-0 bits are "01" or "10", the settings of DHHA13-0 and DHHB13-0 bits are enabled. When DHHPF1-0 bits are "00", HPF block outputs "0" data.

DMLPF1-0: DVLC Middle Frequency Range LPF Coefficient Setting Enable (Table 55)
00: Disable (default)
01: 1st order LPF
10: 2nd order LPF
11: N/A
When DMLPF1-0 bits are "01" or "10", the settings of DMLA13-0 and DMLB13-0 bits are enabled. When DMLPF1-0 bits are "00", the audio data passes DVLC middle frequency range of the LPF by 0dB gain.

DMHPF1-0: DVLC Middle Frequency Range HPF Coefficient Setting Enable (Table 54)
00: Disable (default)
01: 1st order HPF
10: 2nd order HPF
11: N/A
When DMHPF1-0 bits are "01" or "10", the setting of DMHA13-0 and DMHB13-0 bits are enabled. When DMHPF1-0 bits are "00", the audio data passes DVLC middle frequency range of the HPF by 0dB gain.

DLLPF1-0: DVLC Low Frequency Range LPF Coefficient Setting Enable (Table 50)
00: Disable (default)
01: 1st order LPF
10: 2nd order LPF
11: N/A
When DLLPF1-0 bits are "01" or "10", the settings of DLLA13-0 and DLLB13-0 bits are enabled. When DLLPF1-0 bits are "00", LPF block outputs "0" data.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
61H	DVLC Mode Control	DVRGAIN2	DVRGAIN1	DVRGAIN0	DVLMAT2	DVLMAT1	DVLMAT0	DAF1	DAF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	1	0	1	1	1	1

DAF1-0: Moving Avarage Parameter Setting for DVLC (Table 63)
Default: "11" (Default: 2048/fs)

DVLMAT2-0: DVLC Attenuation Speed Setting (Table 64)
Default: "011"

DVRGAIN2-0: DVLC Recovery Speed Setting (Table 65)
Default: "011"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
62H	DVLCL Curve X1	0	0	VL1X5	VL1X4	VL1X3	VL1X2	VL1X1	VL1X0
63H	DVLCL Curve Y1	0	0	VL1Y5	VL1Y4	VL1Y3	VL1Y2	VL1Y1	VL1Y0
64H	DVLCL Curve X2	0	0	VL2X5	VL2X4	VL2X3	VL2X2	VL2X1	VL2X0
65H	DVLCL Curve Y2	0	0	VL2Y5	VL2Y4	VL2Y3	VL2Y2	VL2Y1	VL2Y0
66H	DVLCL Curve X3	0	0	0	VL3X4	VL3X3	VL3X2	VL3X1	VL3X0
67H	DVLCL Curve Y3	0	0	0	VL3Y4	VL3Y3	VL3Y2	VL3Y1	VL3Y0
68H	DVLCL Slope 1	0	L1G6	L1G5	L1G4	L1G3	L1G2	L1G1	L1G0
69H	DVLCL Slope 2	0	L2G6	L2G5	L2G4	L2G3	L2G2	L2G1	L2G0
6AH	DVLCL Slope 3	0	L3G6	L3G5	L3G4	L3G3	L3G2	L3G1	L3G0
6BH	DVLCL Slope 4	0	L4G6	L4G5	L4G4	L4G3	L4G2	L4G1	L4G0
6CH	DVLCM Curve X1	0	0	VM1X5	VM1X4	VM1X3	VM1X2	VM1X1	VM1X0
6DH	DVLCM Curve Y1	0	0	VM1Y5	VM1Y4	VM1Y3	VM1Y2	VM1Y1	VM1Y0
6EH	DVLCM Curve X2	0	0	VM2X5	VM2X4	VM2X3	VM2X2	VM2X1	VM2X0
6FH	DVLCM Curve Y2	0	0	VM2Y5	VM2Y4	VM2Y3	VM2Y2	VM2Y1	VM2Y0
70H	DVLCM Curve X3	0	0	0	VM3X4	VM3X3	VM3X2	VM3X1	VM3X0
71H	DVLCM Curve Y3	0	0	0	VM3Y4	VM3Y3	VM3Y2	VM3Y1	VM3Y0
72H	DVLCM Slope 1	0	M1G6	M1G5	M1G4	M1G3	M1G2	M1G1	M1G0
73H	DVLCM Slope 2	0	M2G6	M2G5	M2G4	M2G3	M2G2	M2G1	M2G0
74H	DVLCM Slope 3	0	M3G6	M3G5	M3G4	M3G3	M3G2	M3G1	M3G0
75H	DVLCM Slope 4	0	M4G6	M4G5	M4G4	M4G3	M4G2	M4G1	M4G0
76H	DVLCH Curve X1	0	0	VH1X5	VH1X4	VH1X3	VH1X2	VH1X1	VH1X0
77H	DVLCH Curve Y1	0	0	VH1Y5	VH1Y4	VH1Y3	VH1Y2	VH1Y1	VH1Y0
78H	DVLCH Curve X2	0	0	VH2X5	VH2X4	VH2X3	VH2X2	VH2X1	VH2X0
79H	DVLCH Curve Y2	0	0	VH2Y5	VH2Y4	VH2Y3	VH2Y2	VH2Y1	VH2Y0
7AH	DVLCH Curve X3	0	0	0	VH3X4	VH3X3	VH3X2	VH3X1	VH3X0
7BH	DVLCH Curve Y3	0	0	0	VH3Y4	VH3Y3	VH3Y2	VH3Y1	VH3Y0
7CH	DVLCH Slope 1	0	H1G6	H1G5	H1G4	H1G3	H1G2	H1G1	H1G0
7DH	DVLCH Slope 2	0	H2G6	H2G5	H2G4	H2G3	H2G2	H2G1	H2G0
7EH	DVLCH Slope 3	0	H3G6	H3G5	H3G4	H3G3	H3G2	H3G1	H3G0
7FH	DVLCH Slope 4	0	H4G6	H4G5	H4G4	H4G3	H4G2	H4G1	H4G0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

VL1X5-0, VL2X5-0, VL3X4-0: Input Gain Setting of Low Range DVLC Point (Table 51, Table 52)
Default: “00H” (0dB)

VL1Y5-0, VL2Y5-0, VL3Y4-0: Output Gain Setting of Low Range DVLC Point (Table 51, Table 52)
Default: “00H” (0dB)

L1G6-0, L2G6-0, L3G6-0, L4G6-0: DVLC Slope Setting of Low Range (Table 53)
Default: “00H”

VM1X5-0, VM2X5-0, VM3X4-0: Input Gain Setting of Middle Range DVLC Point (Table 51, Table 52)
Default: “00H” (0dB)

VM1Y5-0, VM2Y5-0, VM3Y4-0: Output Gain Setting of Middle Range DVLC Point (Table 51, Table 52)
Default: “00H” (0dB)

M1G6-0, M2G6-0, M3G6-0, M4G6-0: DVLC Slope Setting of Middle Range (Table 53)
Default: “00H”

VH1X5-0, VH2X5-0, VH3X4-0: Input Gain Setting of High Range DVLC Point (Table 51, Table 52)
Default: “00H” (0dB)

VH1Y5-0, VH2Y5-0, VH3Y4-0: Output Gain Setting of High Range DVLC Point (Table 51, Table 52)
Default: “00H” (0dB)

H1G6-0, H2G6-0, H3G6-0, H4G6-0: DVLC Slope Setting of High Range (Table 53)
Default: “00H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
80H	DVLCL LPF Co-efficient 0	DLLA7	DLLA6	DLLA5	DLLA4	DLLA3	DLLA2	DLLA1	DLLA0
81H	DVLCL LPF Co-efficient 1	0	0	DLLA13	DLLA12	DLLA11	DLLA10	DLLA9	DLLA8
82H	DVLCL LPF Co-efficient 2	DLLB7	DLLB6	DLLB5	DLLB4	DLLB3	DLLB2	DLLB1	DLLB0
83H	DVLCL LPF Co-efficient 3	0	0	DLLB13	DLLB12	DLLB11	DLLB10	DLLB9	DLLB8
84H	DVLCM HPF Co-efficient 0	DMHA7	DMHA6	DMHA5	DMHA4	DMHA3	DMHA2	DMHA1	DMHA0
85H	DVLCM HPF Co-efficient 1	0	0	DMHA13	DMHA12	DMHA11	DMHA10	DMHA9	DMHA8
86H	DVLCM HPF Co-efficient 2	DMHB7	DMHB6	DMHB5	DMHB4	DMHB3	DMHB2	DMHB1	DMHB0
87H	DVLCM HPF Co-efficient 3	0	0	DMHB13	DMHB12	DMHB11	DMHB10	DMHB9	DMHB8
88H	DVLCM LPF Co-efficient 0	DMLA7	DMLA6	DMLA5	DMLA4	DMLA3	DMLA2	DMLA1	DMLA0
89H	DVLCM LPF Co-efficient 1	0	0	DMLA13	DMLA12	DMLA11	DMLA10	DMLA9	DMLA8
8AH	DVLCM LPF Co-efficient 2	DMLB7	DMLB6	DMLB5	DMLB4	DMLB3	DMLB2	DMLB1	DMLB0
8BH	DVLCM LPF Co-efficient 3	0	0	DMLB13	DMLB12	DMLB11	DMLB10	DMLB9	DMLB8
8CH	DVLCH HPF Co-efficient 0	DHHA7	DHHA6	DHHA5	DHHA4	DHHA3	DHHA2	DHHA1	DHHA0
8DH	DVLCH HPF Co-efficient 1	0	0	DHHA13	DHHA12	DHHA11	DHHA10	DHHA9	DHHA8
8EH	DVLCH HPF Co-efficient 2	DHHB7	DHHB6	DHHB5	DHHB4	DHHB3	DHHB2	DHHB1	DHHB0
8FH	DVLCH HPF Co-efficient 3	0	0	DHHB13	DHHB12	DHHB11	DHHB10	DHHB9	DHHB8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DLLA13-0, DLLB13-0: DVLC Low Frequency Range LPF Coefficient (14bits x 2)
Default: “0000H”

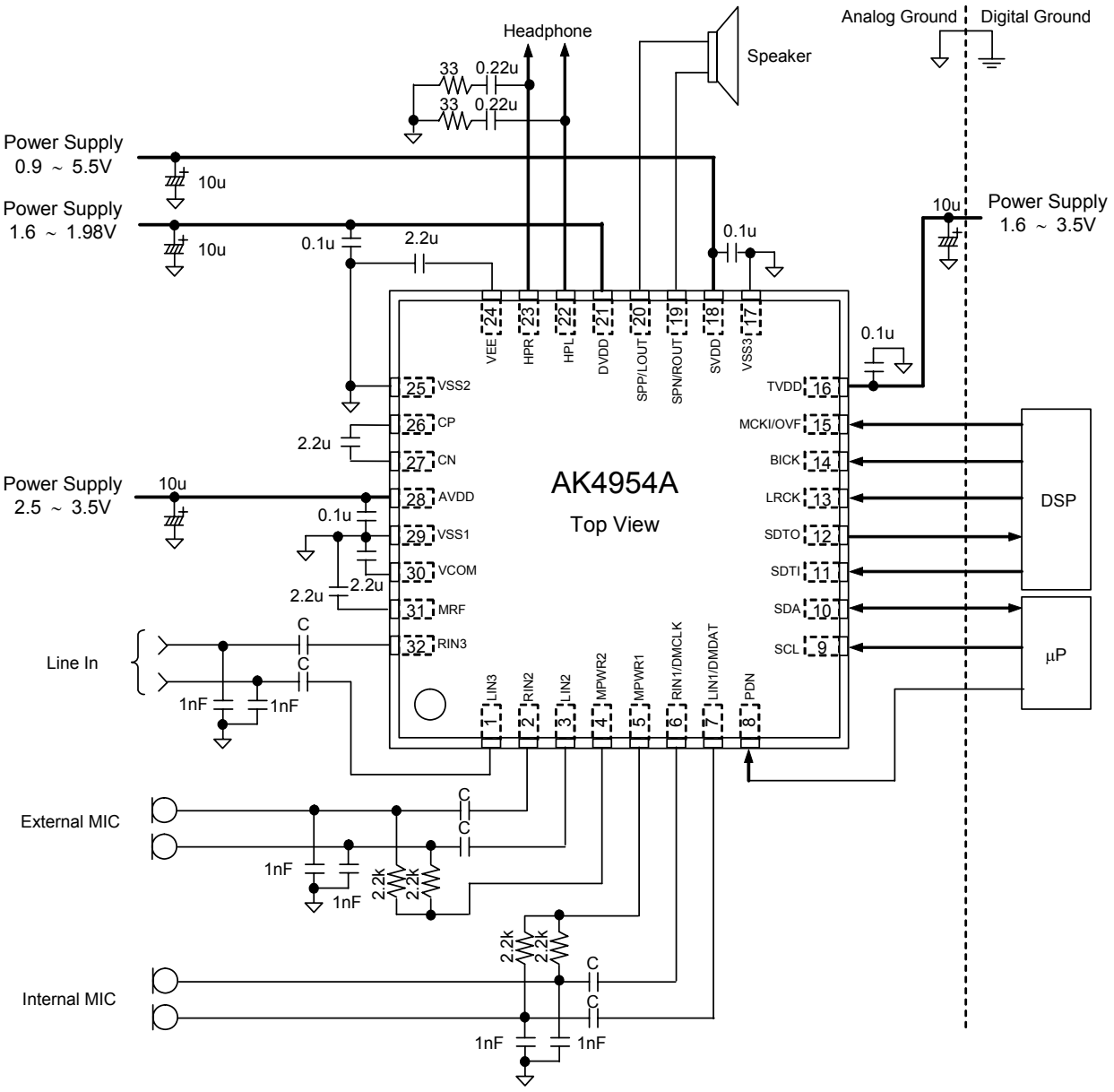
DMHA13-0, DMHB13-0: DVLC Middle Frequency Range HPF Coefficient (14bits x 2)
Default: “0000H”

DMLA13-0, DMLB13-0: DVLC Middle Frequency Range LPF Coefficient (14bits x 2)
Default: “0000H”

DHHA13-0, DHHB13-0: DVLC High Frequency Range HPF Coefficient (14bits x 2)
Default: “0000H”

SYSTEM DESIGN

Figure 63 shows the system connection diagram. An evaluation board (AKD4954A) is available for fast evaluation as well as suggestions for peripheral circuitry.



Notes:

- VSS1, VSS2 and VSS3 of the AK4954A must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- When the AK4954A is used in master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, around 100kΩ pull-up/down resistor must be connected to LRCK and BICK pins of the AK4954A.
- 0.1µF capacitors at power supply pins and 2.2µF capacitors between CP and CN pins, and between VEE and VSS2 pins should be ceramic capacitors. Other capacitors do not have specific types.

Figure 63. System Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4954A requires careful attention to power supply and grounding arrangements. AVDD and SVDD are usually supplied from the system's analog supply, and DVDD and TVDD are supplied from the system's digital power supply. If AVDD, DVDD, TVDD and SVDD are supplied separately, the power-up sequence is not critical. The PDN pin should be held "L" when power supplies are tuning on. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

To avoid pop noise on headphone output and line output when power up/down, the AK4954A should be operated along the following recommended power-up/down sequence.

1) Power-up
- The PDN pin should be held "L" when power supplies are turning on. The AK4954A can be reset by keeping the PDN pin "L" for 1μs or longer after all power supplies are applied and settled.

2) Power-down
- Each of power supplies can be powered OFF after the PDN pin is set to "L".

VSS1, VSS2 and VSS3 of the AK4954A should be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close the power supply pins as possible. Especially, the small value ceramic capacitor is to be closest.

2. Voltage Reference

VCOM is a signal ground of this chip (typ. 0.5 x AVDD). A 2.2μF ±50% electrolytic capacitor attached between the VCOM pin and VSS1 pin eliminates the effects of high frequency noise. It should be connected as close as possible to the VCOM pin. No load current is allowed to be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4954A.

3. Charge Pump

2.2μF±50% capacitors between the CP and CN pins, and the VEE and VSS3 pins should be low ESR ceramic capacitors. These capacitors must be connected as close as possible to the pins. No load current may be drawn from the VEE pin.

4. Analog Inputs

The microphone input is single-ended. The input signal range scales with typ. 0.8 x AVDD Vpp (@ MGAIN = 0dB), centered around the internal common voltage (typ. 0.5 x AVDD). Usually the input signal is AC coupled using a capacitor (2.2μF or less is recommended). If the capacitor is over 2.2μF, pop noises may occur since the ADC output has an offset by a decrement of rising speed of an analog input pin. The cut-off frequency is $fc = 1/(2\pi RC)$. The AK4954A can accept input voltages from VSS1 to AVDD. Connect a 1nF capacitor between each analog input and VSS1 for stabilized characteristics.

5. Analog Outputs

The headphone output is single-ended and centered around VSS (0V). There is no need for AC coupling capacitors. The speaker amplifier (SPP and SPN pins) is BTL output, and they should be connected directly to a speaker. There is no need for AC coupling capacitors. The stereo line outputs (LOUT and ROUT pins) are single-ended and centered on SVDD/2 (typ). These pins must be AC-coupled using a capacitor.

CONTROL SEQUENCE

■ Clock Set up

When any circuits of the AK4954A are powered-up, the clocks must be supplied.

1. PLL Master Mode

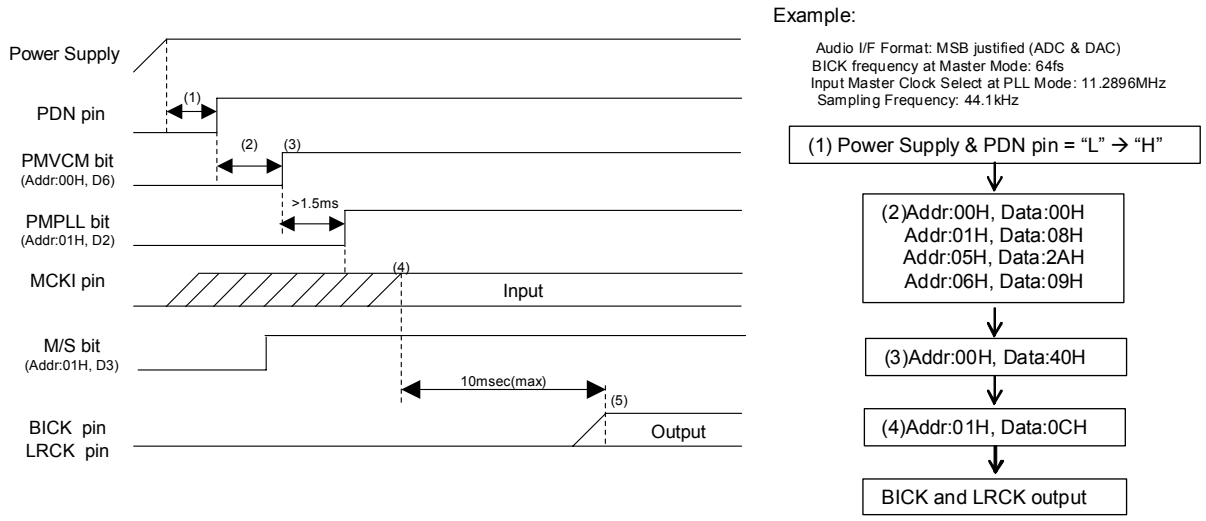


Figure 64. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin "L" → "H".
"L" time of 1μs or more is needed to reset the AK4954A.

(2) Dummy Command (Addr:00H, Data:00H) must be executed before control registers are set. DIF1-0, PLL2-0, FS3-0, BCKO and M/S bits must be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered-up before operating other blocks. Rise-up time of the VCOM pin is 1.5ms (max) when the external capacitance is 2.2μF.

(4) PLL starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source. PLL lock time is 10ms (max).

(5) The AK4954A starts outputting LRCK and BICK clocks after the PLL became stable. Then normal operation starts.

2. PLL Slave Mode (BICK pin)

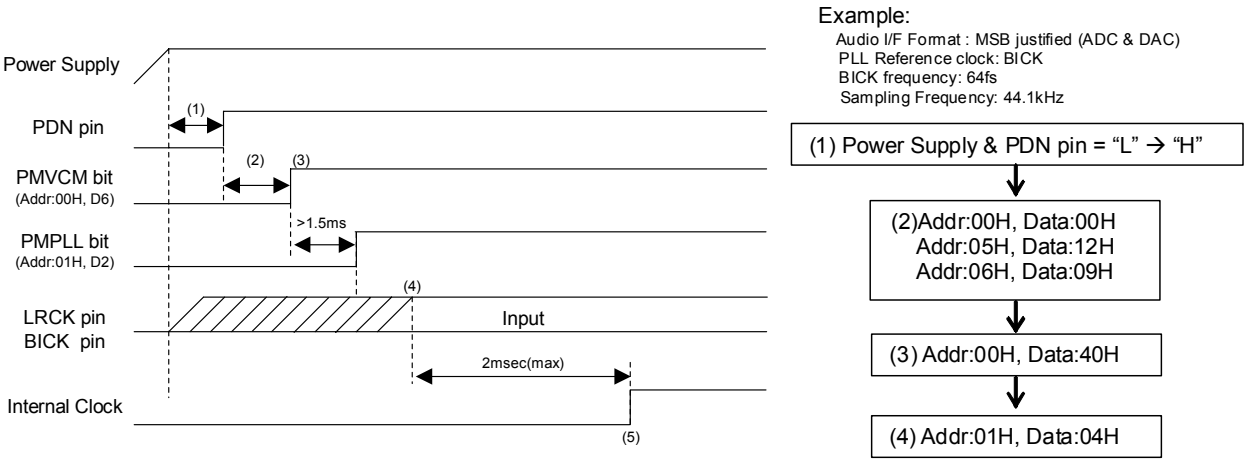


Figure 65. Clock Set Up Sequence (2)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 1μs or more is needed to reset the AK4954A.

(2) Dummy Command (Addr:00H, Data:00H) must be executed before control registers are set. DIF1-0, FS3-0 and PLL2-0 bits must be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered-up before operating other blocks. Rise-up time of the VCOM pin is 1.5ms (max) when the external capacitance is 2.2μF.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (BICK pin) is supplied. PLL lock time is 2ms (max).

(5) Normal operation stats after that the PLL is locked.

3. EXT Slave Mode

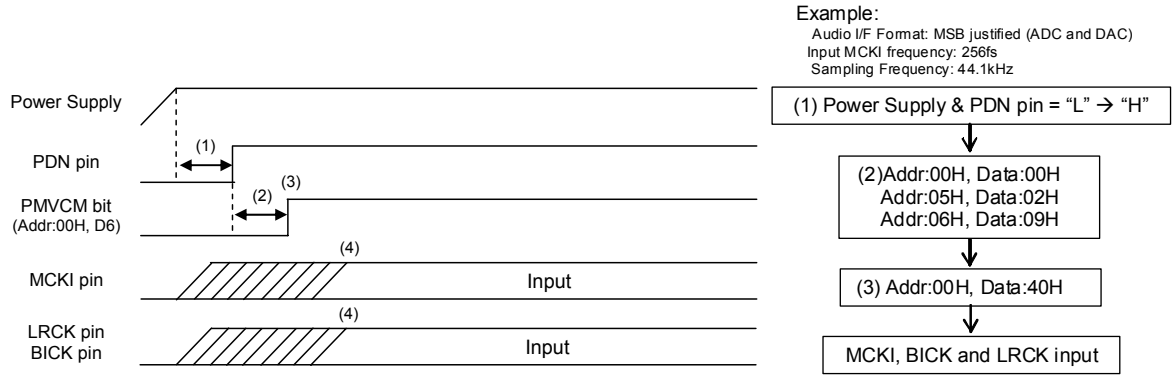


Figure 66. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 1μs or more is needed to reset the AK4954A.

(2) Dummy Command (Addr:00H, Data:00H) must be executed before control registers are set. DIF1-0, CM1-0 and FS3-0 bits must be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered-up before operating other blocks. Rise-up time of the VCOM pin is 1.5ms (max) when the external capacitance is 2.2μF.

(4) MCKI, LRCK and BICK are supplied.

4. EXT Master Mode

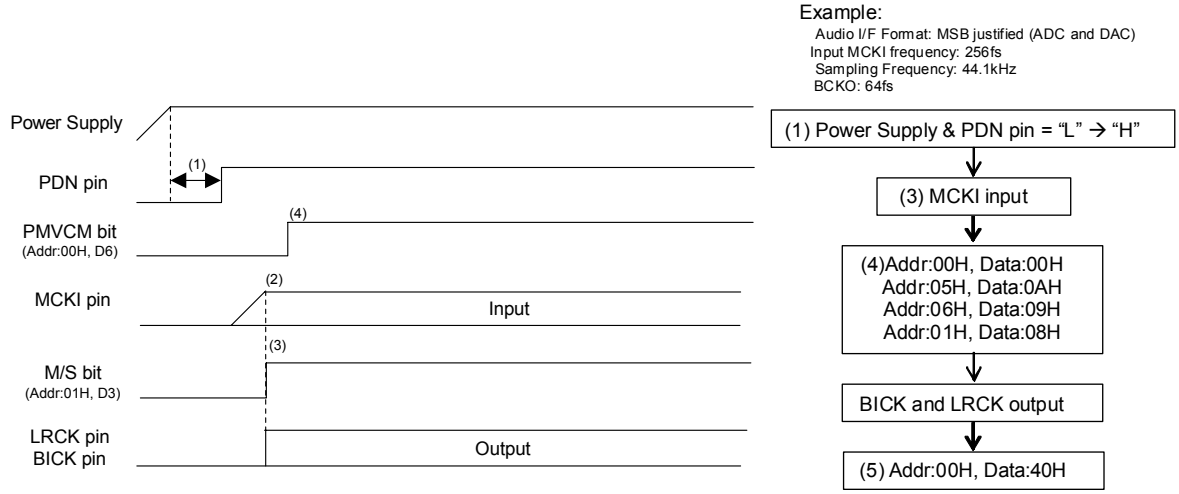


Figure 67. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 1μs or more is needed to reset the AK4954A.

(2) MCKI is supplied.

(3) Dummy Command (Addr:00H, Data:00H) must be executed before control registers are set. After DIF1-0, CM1-0 and FS3-0 bits settings, M/S bit should be set to "1". Then LRCK and BICK are output.

(4) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM must first be powered-up before operating other blocks. Rise-up time of the VCOM pin is 1.5ms (max) when the external capacitance is 2.2μF.

■ Microphone Input Recording (Stereo)

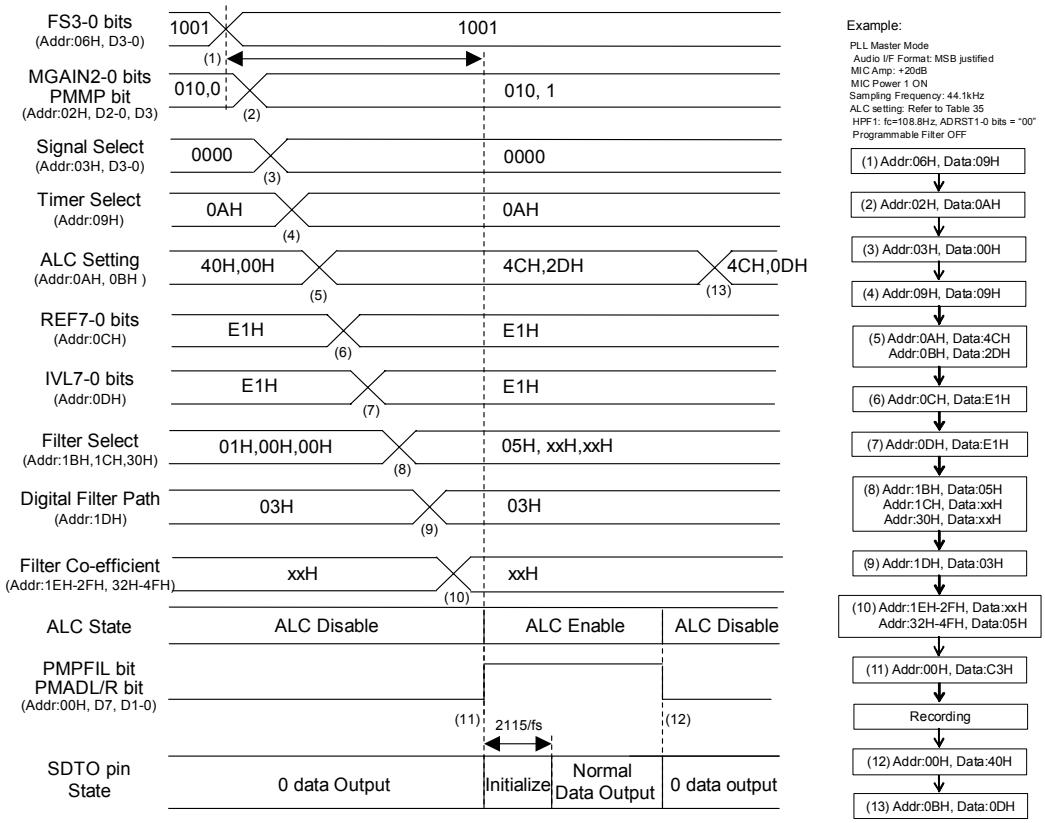


Figure 68. Microphone Input Recording Sequence

<Example>

This sequence is an example of ALC setting at fs=44.1kHz. For changing the parameter of ALC, please refer to "Registers Set-up Sequence in ALC Operation (recording path)".

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up the sampling frequency (FS3-0 bits). When the AK4954A is in PLL mode, Microphone, ADC and Programmable Filter of (11) must be powered-up in consideration of PLL lock time after the sampling frequency is changed.

(2) Set up microphone gain and power up the microphone power supply: MGAIN2-0 bits = "010", PMMP bit = "0" → "1"
Power-up time of microphone is 48ms (max).

(3) Set up input signal. (Addr = 03H)

(4) Set up the Timer: OVTM1-0, OVFL, ADRST1-0 bits (Addr = 09H)

(5) Set up ALC Mode, (Addr = 0AH, 0BH)

(6) Set up REF value of ALC (Addtr = 0CH)

(7) Set up IVOL value of ALC (Addr = 0DH)

(8) Set up Programmable Filter ON/OFF (Addr = 1BH, 1CH, 30H)

(9) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr = 1DH)

(10) Set up Coefficient of the Programmable Filter (Addr: 1EH ~ 2FH, 32H ~ 4FH)

(11) Power up the microphone, ADC and Programmable Filter: PMADL = PMADR =PMPFIL bits = "0" → "1"
The initialization cycle time of ADC is 2115/fs=48ms @ fs=44.1kHz, ADRST1-0 bit = "00". The ADC outputs "0" data during the initialization cycle. After the ALC bit is set to "1", the ALC operation starts from IVOL value of (7).

(12) Power down the microphone, ADC and Programmable Filter: PMADL = PMADR = PMPFIL bits = "1" → "0"

(13) ALC Disable: ALC bit = "1" → "0"

■Digital Microphone Input Recording (Stereo)

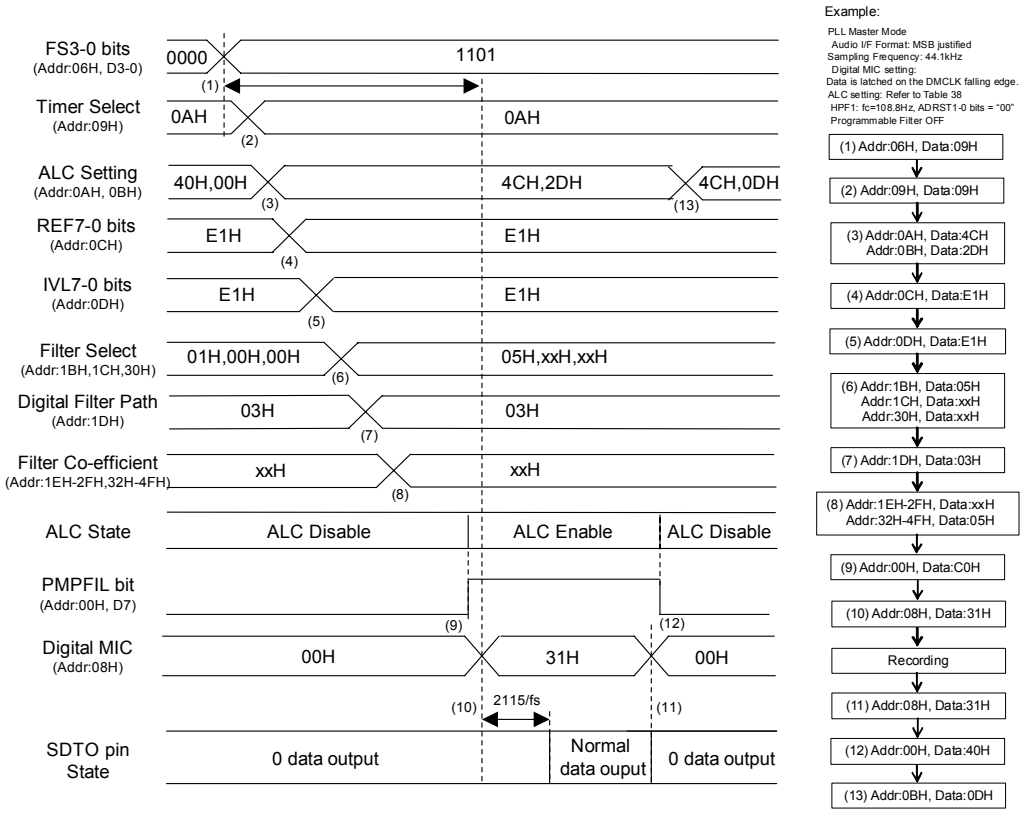


Figure 69. Digital Microphone Input Recording Sequence

<Example>

This sequence is an example of ALC setting at fs=44.1kHz. For changing the parameter of ALC, please refer to "Registers Set-up Sequence in ALC Operation (recording path)".

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up the sampling frequency (FS3-0 bits). When the AK4954A is in PLL mode, digital microphone (10) and Programmable Filter (9) must be powered-up in consideration of PLL lock time after the sampling frequency is changed.
(2) Set up the Timer: OVTM1-0, OVFL, ADRST1-0 bits (Addr = 09H)
(3) Set up ALC Mode, (Addr = 0AH, 0BH)
(4) Set up REF value of ALC (Addtr = 0CH)
(5) Set up IVOL value of ALC (Addr = 0DH)
(6) Set up Programmable Filter ON/OFF (Addr = 1BH, 1CH, 30H)
(7) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr = 1DH)
(8) Set up Coefficient of the Programmable Filter (Addr: 1EH ~ 2FH, 32H ~ 4FH)
(9) Power up the Programmable Filter: PMPFIL bit = "0" → "1"
(10) Set up Digital Microphone and Power up: DMIC bit = "0" → "1", PMDMR = PMDML bits = "0" → "1"
The initialization cycle time of ADC is 2115/fs=48ms @ fs=44.1kHz, ADRST1-0 bit = "00". ADC outputs "0" data during the initialization cycle. After the ALC bit is set to "1", the ALC operation starts from IVOL value of (5).
(11) Power down microphone: PMDMR = PMDMR = PMPFIL bits = "1" → "0"
(12) Power down programmable filter: PMPFIL bit = "1" → "0"
(13) ALC Disable: ALC bit = "1" → "0"

■ Headphone Amplifier Output

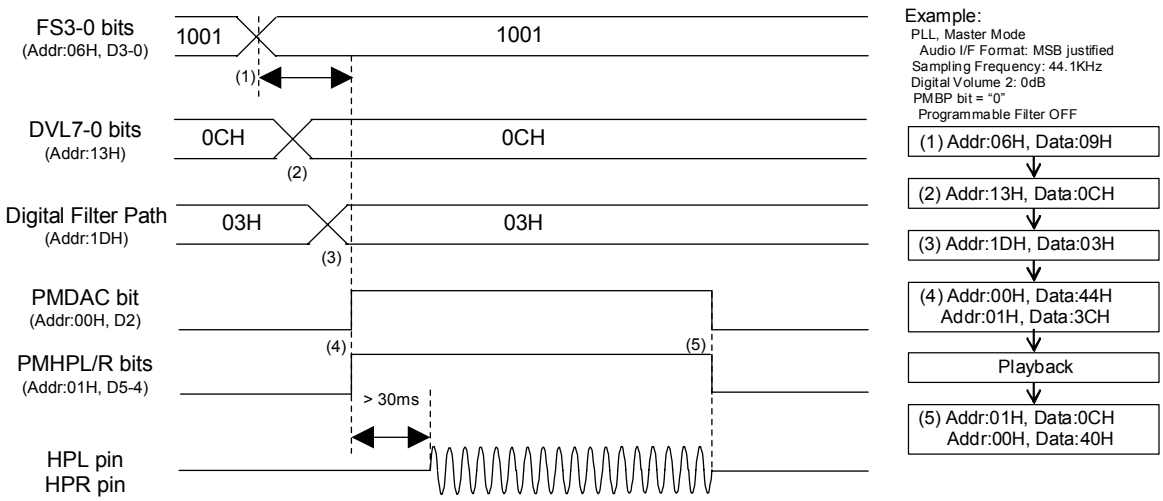


Figure 70. Headphone Amplifier Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

If HPZ bit is "1", write "0" to HPZ bit before the headphone operation starts and set registers in accordance with the control sequence below.

(1) Set up the sampling frequency (FS3-0 bits). When the AK4954A is PLL mode, the Headphone Amplifier and DAC of (4) must be powered-up in consideration of PLL lock time after the sampling frequency is changed.

(2) Set up the digital output volume (Addr = 13H)

(3) Set up Programmable Filter Path: PFDAC, ADCPF and PFSDO bits (Addr = 1DH)

(4) Power up DAC and Headphone Amplifier: PMDAC = PMHPL = PMHPR bits = "0" → "1"
When PMHPL = PMHPR bits = "1", the charge pump circuit is powered-up. The power-up time of Headphone Amplifier block is 30ms (max).

(5) Power down DAC and Headphone Amplifier: PMDAC = PMHPL = PMHPR bits = "1" → "0"

■ Beep Signal Output from Headphone Amplifier

1. Power down DAC → Headphone Amplifier

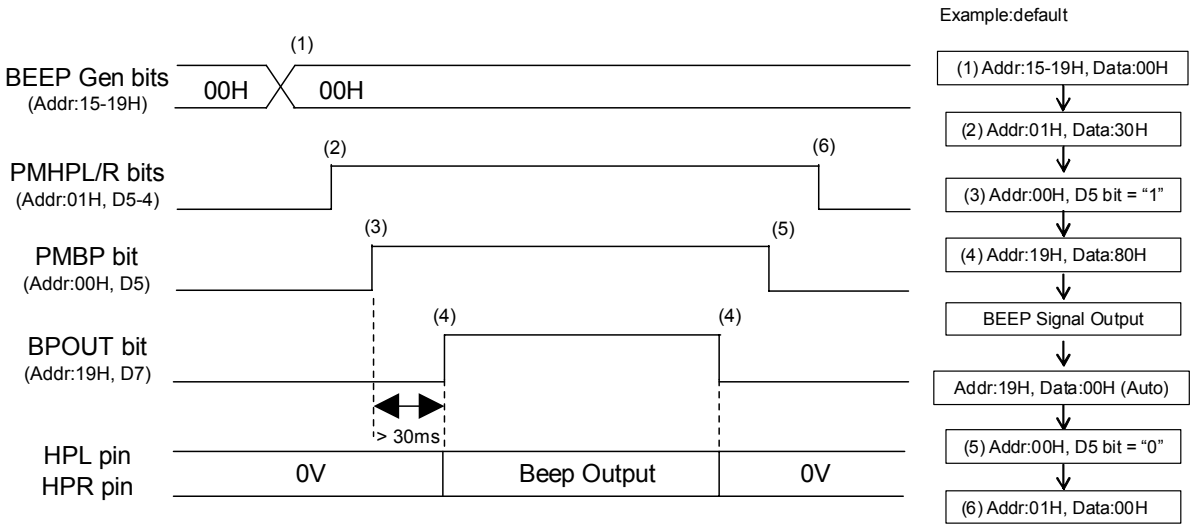


Figure 71. "BEEP Generator → Headphone Amplifier" Output Sequence

<Example>
At first, clocks should be supplied according to "Clock Set Up" sequence.
If HPZ bit is "1", write "0" to HPZ bit before the headphone operation starts and set registers in accordance with the control sequence below.

(1) Set up BEEP Generator (Addr: 15H ~ 19H) (When repeat output time: BPCNT bit = "0")
(2) Power up Headphone Amplifier: PMHPL bit or PMHPR bit = "0" → "1"
(3) Power up BEEP-Generator: PMBP bit = "0" → "1"
Charge pump circuit is powered-up. The power-up time of Headphone Amplifier block is 30ms (max).
(4) BEEP output: BPOUT bit= "0" → "1"
After outputting data particular set times, BPOUT bit automatically goes to "0".
(5) Power down BEEP Generator: PMBP bit = "1" → "0"
(6) Power down Headphone Amplifier: PMHPL bit or PMHPR bit = "1" → "0"

2. Power up DAC → Headphone Amplifier

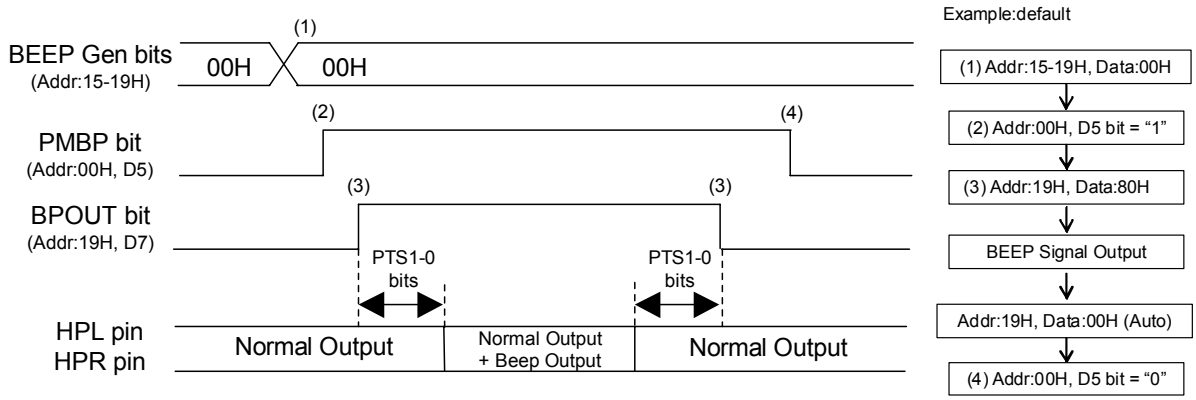


Figure 72. "BEEP Generator → Headphone Amplifier" Output Sequence

<Example>
At first, clocks should be supplied according to "Clock Set Up" sequence, and Headphone Amplifier output should be started according to "Headphone Amplifier Output" sequence.

(1) Set up BEEP Generator (Addr: 15H ~ 19H) (When repeat output time: BPCNT bit = "0")
(2) Power up BEEP Generator: PMBP bit = "0" → "1"
(3) BEEP output: BPOUT bit= "0" → "1"
After the transition time set by PTS1-0 bits, BEEP output starts. BPOUT bit automatically goes to "0" after outputting BEEP for determined number of times by setting.
(4) Power down BEEP Generator: PMBP bit = "1" → "0"

■ Speaker Amplifier Output

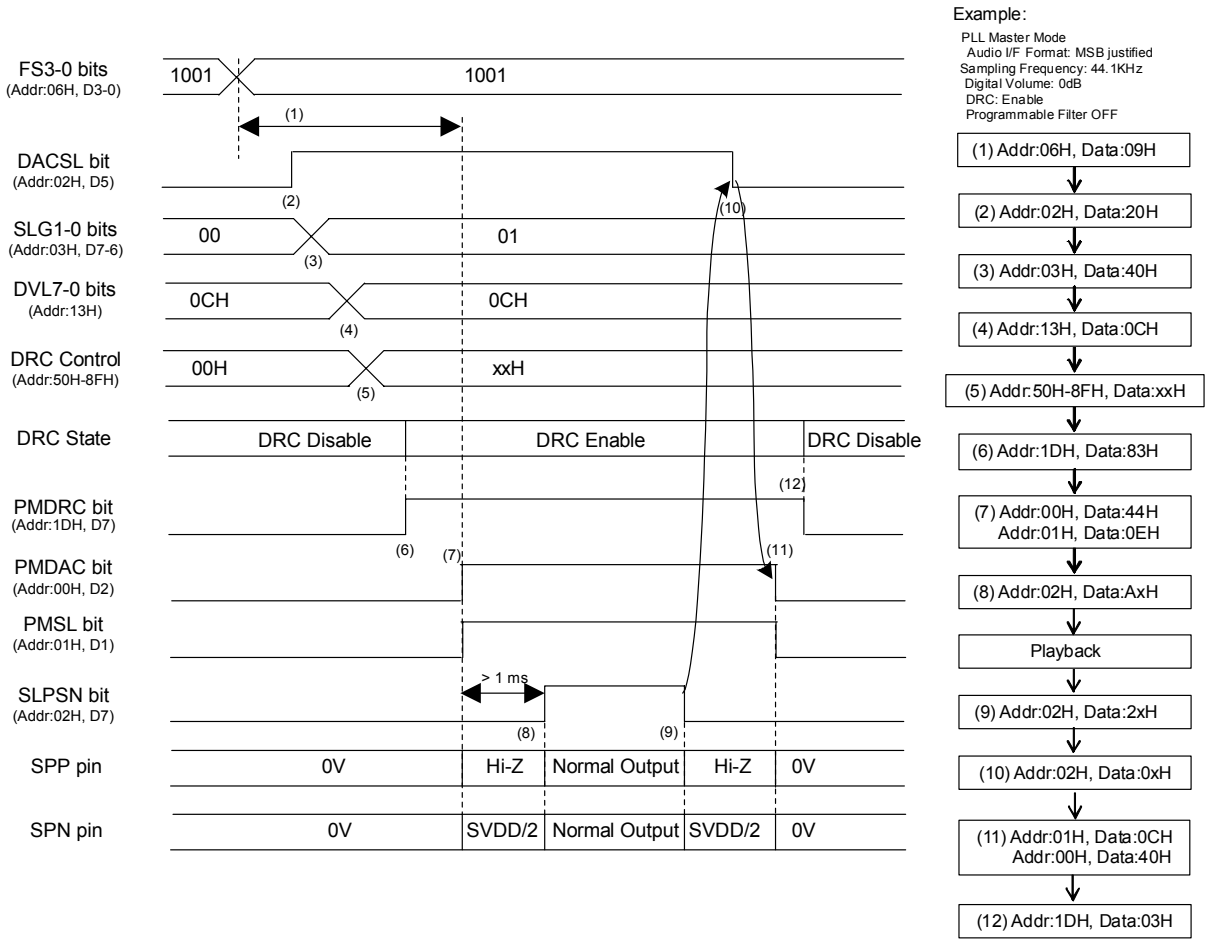


Figure 73. Speaker Amplifier Output Sequence

<Example>

At first, clocks must be supplied according to "Clock Set Up" sequence.

When using HPZ bit to reduce crosstalk to the headphone output, set HPZ bit to "1" first before the speaker operation starts, and then write registers in accordance with the control sequence below.

(1) Set up the sampling frequency (FS3-0 bits). When the AK4954A is PLL mode, DAC and Speaker Amplifier of (7) must be powered-up in consideration of PLL lock time after the sampling frequency is changed.
(2) Set up the path of DAC → SPK Amplifier: DACS bit = "0" → "1"
(3) Set up SPK Amplifier gain: SLG1-0 bits = "00" → "01"
(4) Set up Digital Output Volume Control (Addr = 13H)
(5) Set up DRC Control (Addr = 50H ~ 8FH)
(6) Power up DRC: PMDRC bit = "0" → "1"
(7) Power up DAC and SPK Amplifier: PMDAC = PMSL bits = "0" → "1"
(8) Exit SPK Amplifier power save mode: SLPSN bit = "0" → "1"
(9) Enter SPK Amplifier power save mode: SLPSN bit = "1" → "0"
(10) Set up the path of "DAC → SPK Amplifier": DACSL bit = "1" → "0"
(11) Power down DAC and SPK Amplifier: PMDAC = PMSL bits = "1" → "0"
(12) Power down DRC: PMDRC bit = "1" → "0"

■ Beep Output from Speaker Amplifier

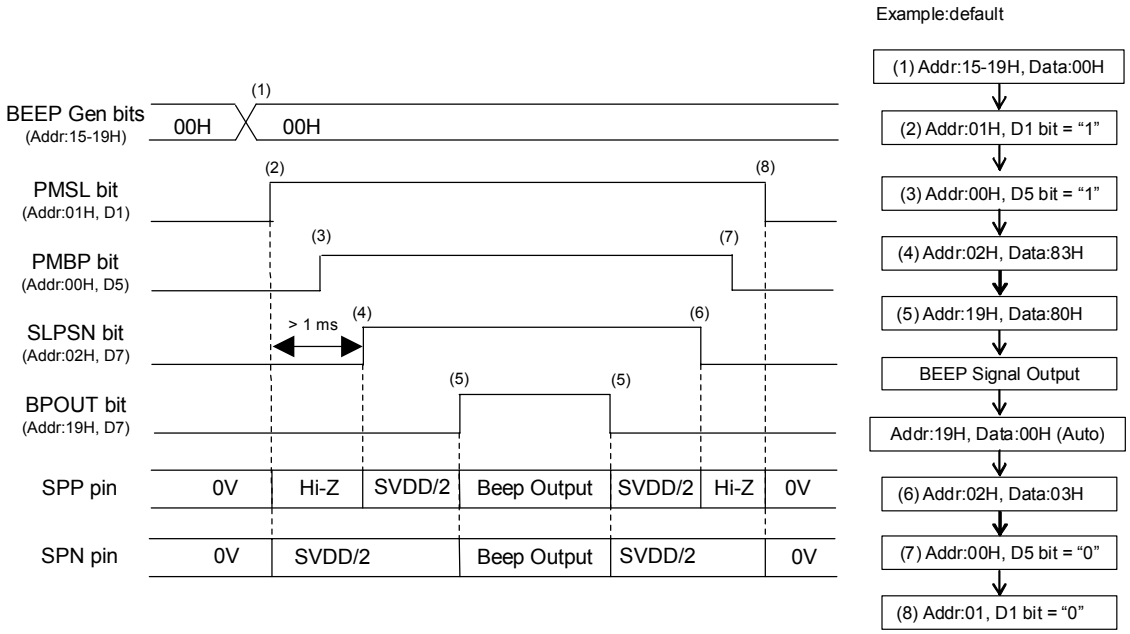


Figure 74. "BEEP Generator → Speaker Amplifier" Output Sequence

<Example>

At first, clocks must be supplied according to "Clock Set Up" sequence.

When using HPZ bit to reduce crosstalk to the headphone output, set HPZ bit to "1" first before the speaker operation starts, and then write registers in accordance with the control sequence below.

(1) Set up BEEP Generator (Addr: 15H ~ 19H) (When repeat output time: BPCNT bit = "0")
(2) Power up Speaker Amplifier: PMSL bit = "0" → "1"
(3) Power up BEEP Generator: PMBP bit = "0" → "1"
(4) Exit power-save-mode of Speaker Amplifier: SLPSN bit = "0" → "1"
(5) BEEP output: BPOUT bit= "0" → "1"
After outputting BEEP for determined number of times, BPOUT bit automatically goes to "0".
(6) Enter Speaker Amplifier power save mode: SLPSN bit = "1" → "0"
(7) Power down BEEP Generator: PMBP bit = "1" → "0"
(8) Power down Speaker Amplifier: PMSL bit = "1" → "0"

■ Stop of Clock

When any circuits of the AK4954A are powered-up, the clocks must be supplied.

1. PLL Master Mode

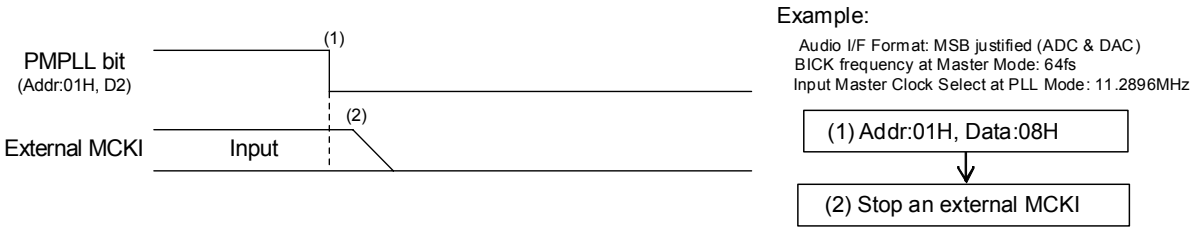


Figure 75. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external master clock.

2. PLL Slave Mode (BICK pin)

Figure 76. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop external clocks.

3. EXT Slave Mode

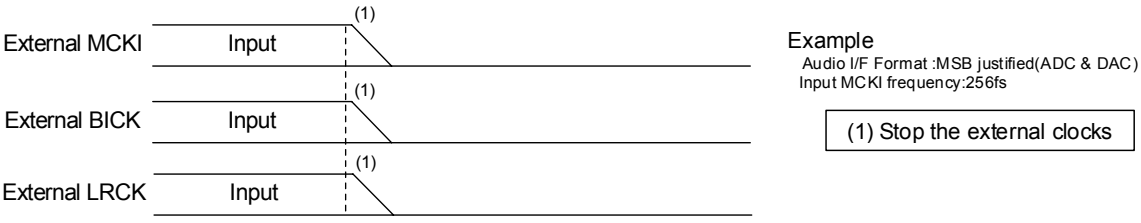


Figure 77. Clock Stopping Sequence (3)

<Example>
(1) Stop external clocks.

4. EXT Master Mode

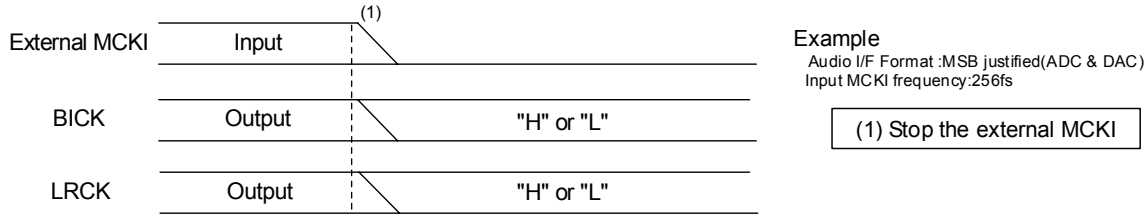


Figure 78. Clock Stopping Sequence (4)

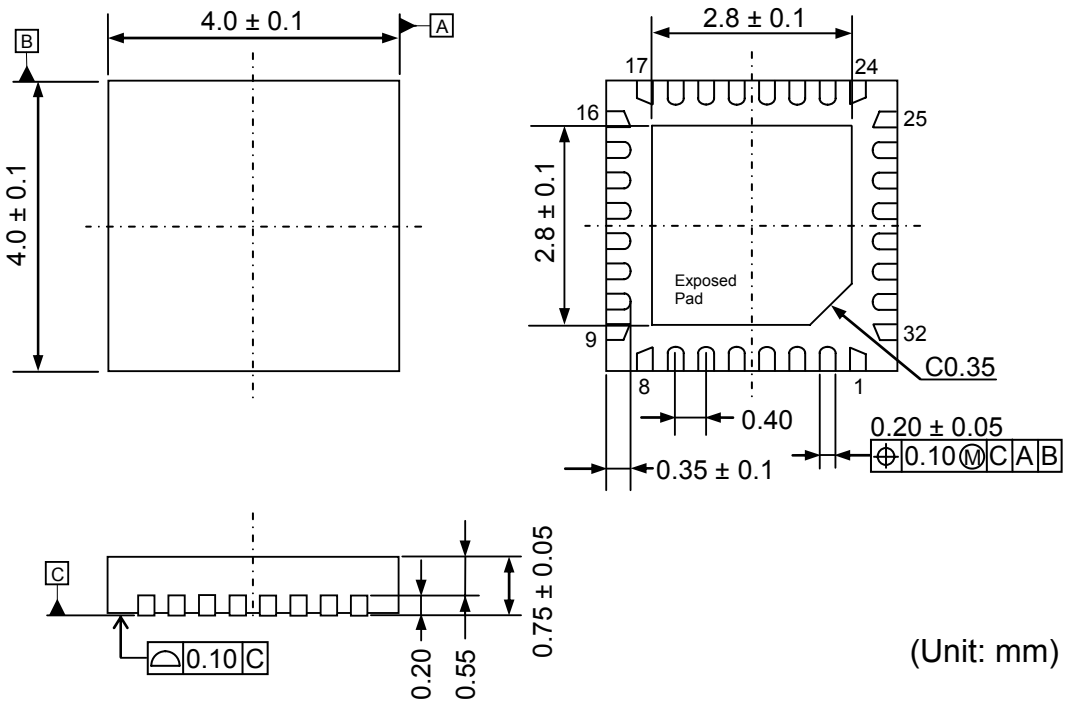
<Example>
(1) Stop the external MCKI. BICK and LRCK are fixed to “H” or “L”.

■ Power-down

Power supply current can not be shut down completely by stopping clocks and setting PMVCM bit = “0”. Power supply current can be shut down (typ. 0μA) by stopping clocks and setting the PDN pin = “L”. When the PDN pin = “L”, all registers are initialized.

PACKAGE

32pin QFN

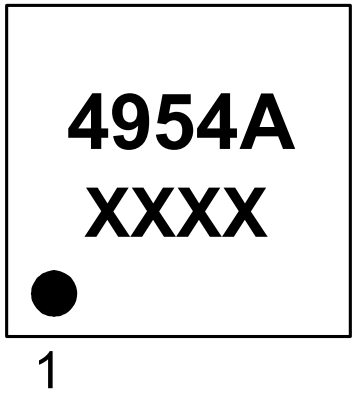


Note: The exposed pad on the bottom surface of the package must be connected to the ground.

■ Material & Lead finish

Package molding compound: Epoxy Resin, Halogen (Br and Cl) free
Lead frame material: Cu Alloy
Lead frame surface treatment: Solder (Pb free) plate

MARKING



XXXX: Date code (4 digit)
Pin #1 indication

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page/Line	Contents
13/06/07	00	First Edition		