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Kind regards,

Team Nexperia

74ALVCH16952

16-bit registered transceiver; 3-state

Rev. 02 — 27 April 2006 Product data sheet

1. General description

The 74ALVCH16952 consists of two sections, each containing a dual octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the clock (nCPAB and nCPBA) provided that the clock enable ($n\overline{CEAB}$ and $n\overline{CEBA}$) is LOW. The data is then present at the output buffers, but is only accessible when the output enable input ($n\overline{OEAB}$ and $n\overline{OEBA}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

2. Features

- CMOS low-power consumption
- Multibyte flow-through pinout architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines at 85 °C
- Complies with JEDEC standard JESD8-B

3. Quick reference data

Table 1. Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay					
	nCPBA to nAn; nCPAB to nBn	V_{CC} = 3.3 V; C_L = 50 pF	-	3.2	-	ns
		V_{CC} = 2.5 V; C_L = 30 pF	-	3.2	-	ns
f_{max}	maximum input clock frequency	V_{CC} = 3.3 V	-	350	-	MHz
C_i	input capacitance		-	3.0	-	pF
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} [1]	-	30	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

PHILIPS

4. Ordering information

Table 2. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
DGG	–40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

5. Functional diagram

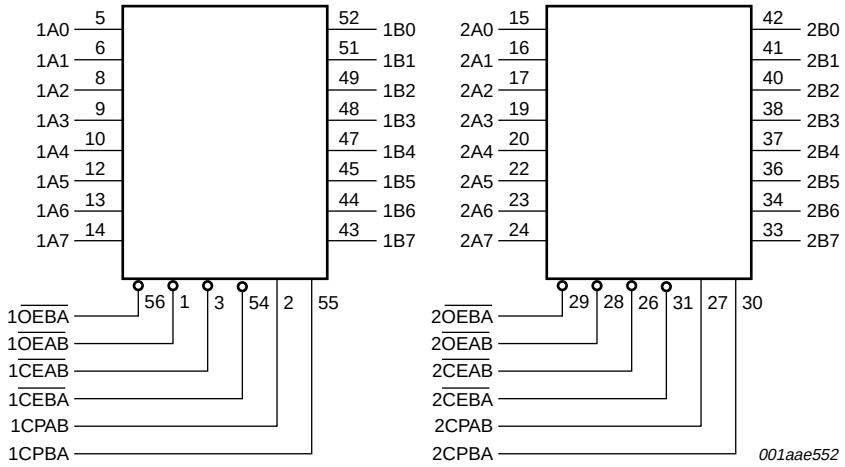


Fig 1. Logic symbol

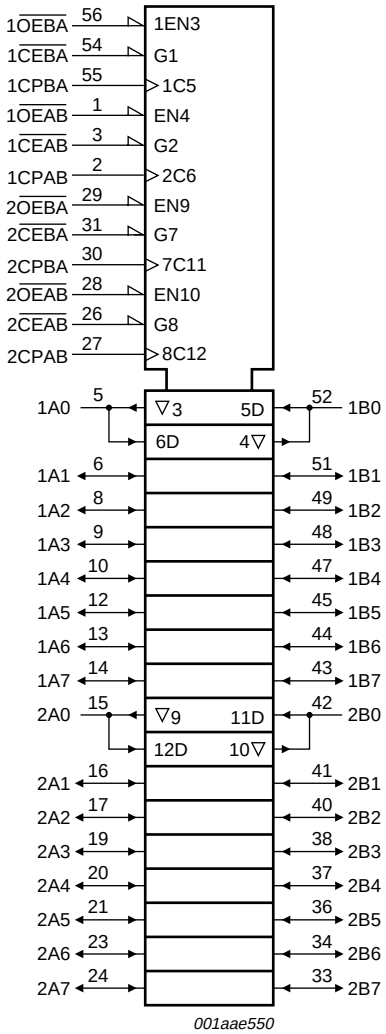


Fig 2. IEC logic symbol

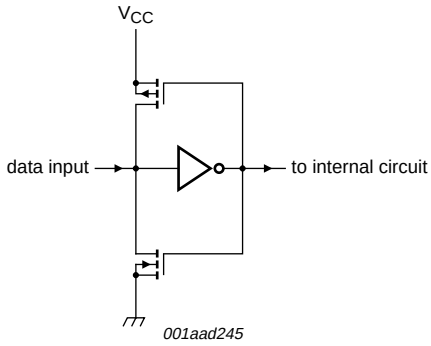


Fig 3. Bus hold circuit

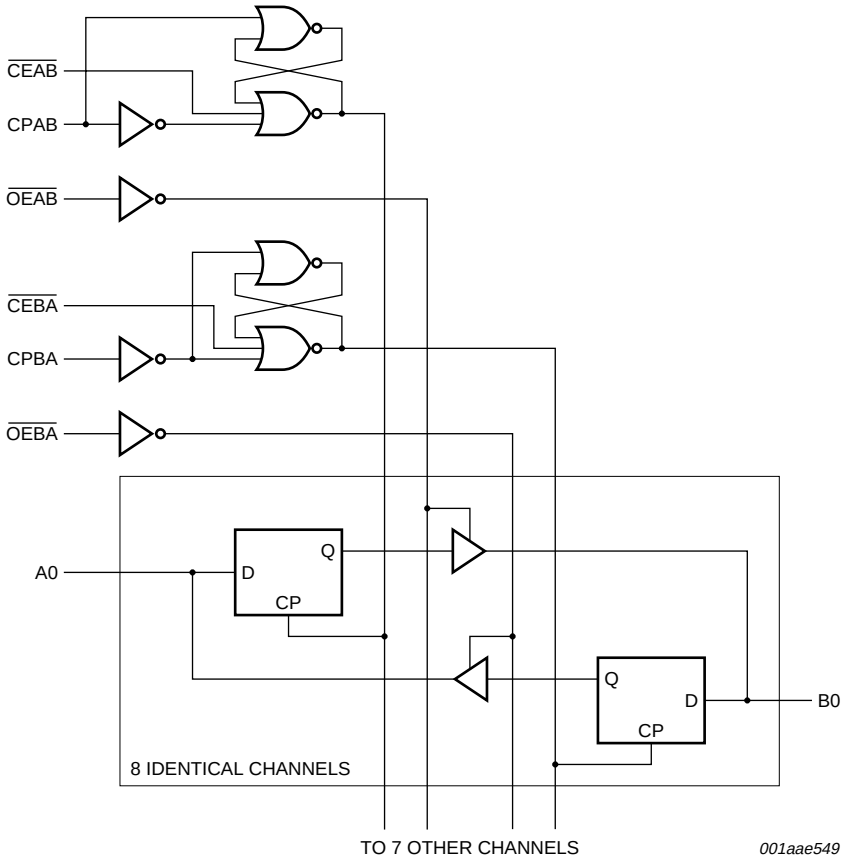


Fig 4. Schematic diagram (one section)

6. Pinning information

6.1 Pinning

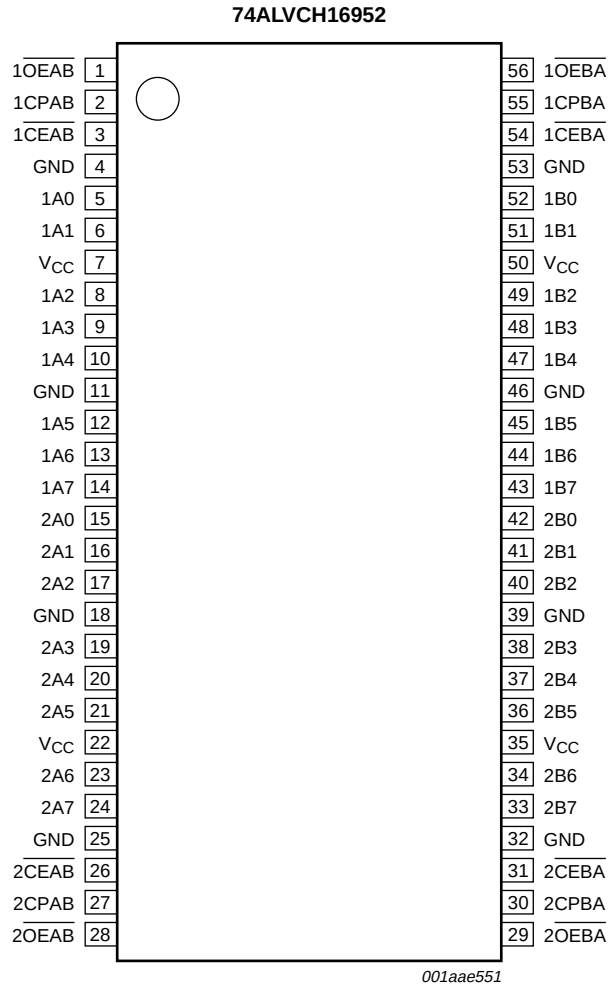


Fig 5. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$1\overline{OEAB}$	1	output enable input (active LOW)
1CPAB	2	clock pulse input (active rising edge)
$1\overline{CEAB}$	3	clock enable input (active LOW)
GND	4	ground (0 V)
1A0	5	data input or output 1A0
1A1	6	data input or output 1A1
V_{CC}	7	supply voltage

Table 3. Pin description *…continued*

Symbol	Pin	Description
1A2	8	data input or output 1A2
1A3	9	data input or output 1A3
1A4	10	data input or output 1A4
GND	11	ground (0 V)
1A5	12	data input or output 1A5
1A6	13	data input or output 1A6
1A7	14	data input or output 1A7
2A0	15	data input or output 2A0
2A1	16	data input or output 2A1
2A2	17	data input or output 2A2
GND	18	ground (0 V)
2A3	19	data input or output 2A3
2A4	20	data input or output 2A4
2A5	21	data input or output 2A5
V_{CC}	22	supply voltage
2A6	23	data input or output 2A6
2A7	24	data input or output 2A7
GND	25	ground (0 V)
$2\overline{CEAB}$	26	clock enable input (active LOW)
2CPAB	27	clock pulse input (active rising edge)
$2\overline{OEAB}$	28	output enable input (active LOW)
$2\overline{OEBA}$	29	output enable input (active LOW)
2CPBA	30	clock pulse input (active rising edge)
$2\overline{CEBA}$	31	clock enable input (active LOW)
GND	32	ground (0 V)
2B7	33	data input or output 2B7
2B6	34	data input or output 2B6
V_{CC}	35	supply voltage
2B5	36	data input or output 2B5
2B4	37	data input or output 2B4
2B3	38	data input or output 2B3
GND	39	ground (0 V)
2B2	40	data input or output 2B2
2B1	41	data input or output 2B1
2B0	42	data input/output 2B0
1B7	43	data input or output 1B7
1B6	44	data input or output 1B6
1B5	45	data input or output 1B5
GND	46	ground (0 V)
1B4	47	data input or output 1B4
1B3	48	data input or output 1B3

Table 3. Pin description *…continued*

Symbol	Pin	Description
1B2	49	data input or output 1B2
V_{CC}	50	supply voltage
1B1	51	data input or output 1B1
1B0	52	data input or output 1B0
GND	53	ground (0 V)
$1\overline{CEBA}$	54	clock enable input (active LOW)
1CPBA	55	clock pulse input (active rising edge)
$1\overline{OEBA}$	56	output enable input (active LOW)

7. Functional description

7.1 Function table

Table 4. Function table[1][2]

Operating mode	Control			Input	Internal nQn	Output
	$n\overline{OEAB}$	$n\overline{CEAB}$	nCPAB	nAn		nBn
Hold	L	H	X	X	NC	NC
Load and output enable	L	L	↑	L	L	L
				H	H	H
Load and output disable	H	L	↑	L	L	Z
				H	H	Z

[1] A-to-B data flow is shown; B-to-A data flow is similar, but uses signals $n\overline{OEBA}$, $n\overline{CEBA}$ and nCPBA

[2] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH transition;
X = don't care;
Z = high impedance OFF-state;
NC = no change.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
V_I	input voltage	control pins	[1]	–0.5	+4.6	V
		data inputs	[1]	–0.5	V_{CC} + 0.5	V
V_O	output voltage		[1]	–0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V		-	–50	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	quiescent supply current			-	100	mA
I_{GND}	ground current			-	–100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	600	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 55 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	C_L = 30 pF	[1]	2.3	-	2.7	V
		C_L = 50 pF	[1]	3.0	-	3.6	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature	in free-air		–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V		0	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V		0	-	10	ns/V

[1] Maximum speed performance.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C[1]							
V_{IH}	HIGH-state input voltage	V_{CC} = 2.3 V to 2.7 V		1.7	1.2	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	1.5	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.3 V to 2.7 V		-	1.2	0.7	V
		V_{CC} = 2.7 V to 3.6 V		-	1.5	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_{OH} = −100 µA; V_{CC} = 2.3 V to 3.6 V		V_{CC} − 0.2	V_{CC}	-	V
		I_{OH} = −6 mA; V_{CC} = 2.3 V		V_{CC} − 0.3	V_{CC} − 0.08	-	V
		I_{OH} = −12 mA; V_{CC} = 2.3 V		V_{CC} − 0.6	V_{CC} − 0.26	-	V
		I_{OH} = −12 mA; V_{CC} = 2.7 V		V_{CC} − 0.5	V_{CC} − 0.14	-	V
		I_{OH} = −12 mA; V_{CC} = 3.0 V		V_{CC} − 0.6	V_{CC} − 0.09	-	V
		I_{OH} = −24 mA; V_{CC} = 3.0 V		V_{CC} − 1.0	V_{CC} − 0.28	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_{OL} = 100 µA; V_{CC} = 2.3 V to 3.6 V		-	GND	0.20	V
		I_{OL} = 6 mA; V_{CC} = 2.3 V		-	0.07	0.40	V
		I_{OL} = 12 mA; V_{CC} = 2.3 V		-	0.15	0.70	V
		I_{OL} = 12 mA; V_{CC} = 2.7 V		-	0.14	0.40	V
		I_{OL} = 24 mA; V_{CC} = 3.0 V		-	0.27	0.55	V
I_{LI}	input leakage current	V_{CC} = 2.3 V to 3.6 V; $V_I = V_{CC}$ or GND		-	0.1	5	µA
I_{OZ}	off-state output current	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		-	0.1	10	µA
I_{CC}	quiescent supply current	V_{CC} = 2.3 V to 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A		-	0.2	40	µA
ΔI_{CC}	additional quiescent supply current	V_{CC} = 2.3 V to 3.6 V; $V_I = V_{CC}$ − 0.6 V; I_O = 0 A		-	150	750	µA
I_{BHL}	bus hold LOW sustaining current	V_{CC} = 2.3 V; V_I = 0.7 V	[2]	45	-	-	µA
		V_{CC} = 3.0 V; V_I = 0.8 V	[2]	75	150	-	µA
I_{BHH}	bus hold HIGH sustaining current	V_{CC} = 2.3 V; V_I = 1.7 V	[2]	−45	-	-	µA
		V_{CC} = 3.0 V; V_I = 2.0 V	[2]	−75	−175	-	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V	[2]	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V	[2]	−500	-	-	µA
C_i	input capacitance			-	3.0	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

[2] Valid for data inputs of bus hold parts.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay nCPBA to nAn; nCPAB to nBn	see Figure 6					
		V_{CC} = 2.3 V to 2.7 V		1.0	3.2	4.1	ns
		V_{CC} = 2.7 V		1.0	-	4.6	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	3.2	3.9	ns
t_{PZH}, t_{PZL}	3-state output enable time $n\overline{OEBA}$ to nAn; $n\overline{OEAB}$ to nBn	see Figure 8					
		V_{CC} = 2.3 V to 2.7 V		1.0	-	5.4	ns
		V_{CC} = 2.7 V		1.0	-	5.3	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	4.4	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $n\overline{OEBA}$ to nAn; $n\overline{OEAB}$ to nBn	see Figure 8					
		V_{CC} = 2.3 V to 2.7 V		1.0	-	5.3	ns
		V_{CC} = 2.7 V		1.4	-	4.4	ns
		V_{CC} = 3.0 V to 3.6 V		1.1	-	4.0	ns
t_W	pulse width	see Figure 6					
	HIGH or LOW nCPAB; nCPBA	V_{CC} = 2.3 V to 2.7 V		3.3	-	-	ns
		V_{CC} = 2.7 V		3.3	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		3.3	-	-	ns
t_{su}	setup time	see Figure 7					
	nAn to nCPAB or nBn to nCPBA	V_{CC} = 2.3 V to 2.7 V		1.7	-	-	ns
		V_{CC} = 2.7 V		1.9	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	-	-	ns
	$n\overline{CEAB}$ to nCPAB or $n\overline{CEBA}$ to nCPBA	V_{CC} = 2.3 V to 2.7 V		1.2	-	-	ns
		V_{CC} = 2.7 V		1.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	-	ns
t_h	hold time	see Figure 7					
	nAn to nCPAB or nBn to nCPBA	V_{CC} = 2.3 V to 2.7 V		0.6	-	-	ns
		V_{CC} = 2.7 V		0.6	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		0.8	-	-	ns
	$n\overline{CEAB}$ to nCPAB or $n\overline{CEBA}$ to nCPBA	V_{CC} = 2.3 V to 2.7 V		1.1	-	-	ns
		V_{CC} = 2.7 V		0.9	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.1	-	-	ns
f_{max}	maximum clock pulse frequency	see Figure 6					
		V_{CC} = 2.3 V to 2.7 V		150	350	-	MHz
		V_{CC} = 2.7 V		150	350	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	350	-	MHz
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}	[2]	-	30	-	pF

[1] Typical values are measured at nominal supply voltage and at T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

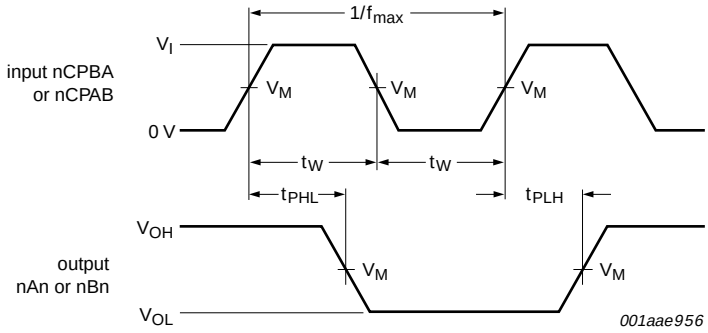
C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

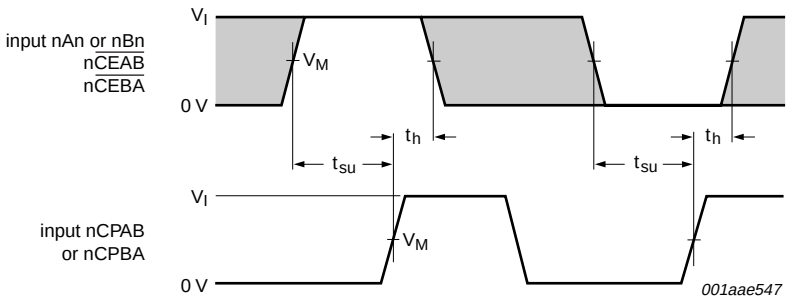
12. Waveforms



Measurements points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

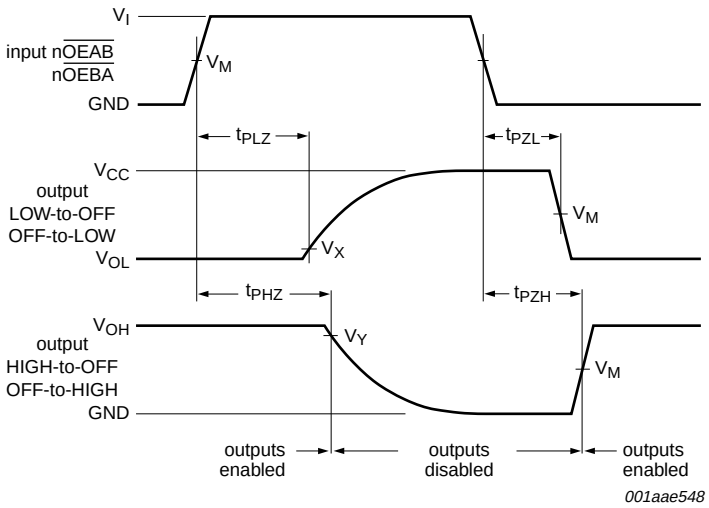
Fig 6. Propagation delay clock input (nCPAB, nCPBA) to output (nBn, nAn), clock pulse width and maximum clock pulse frequency



Measurements points are given in Table 9.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 7. Setup and hold times



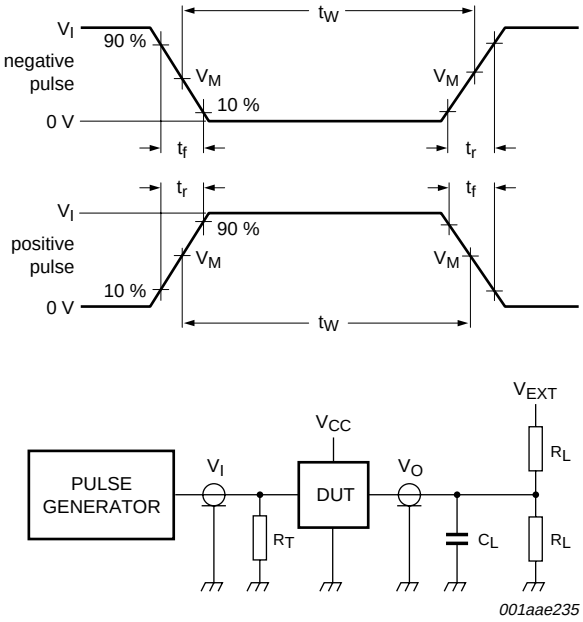
Measurements points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 8. 3-state enable and disable time

Table 9. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	V_{CC}	0.5 V	0.5 V	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistor.

V_{EXT} = Test voltage for switching times.

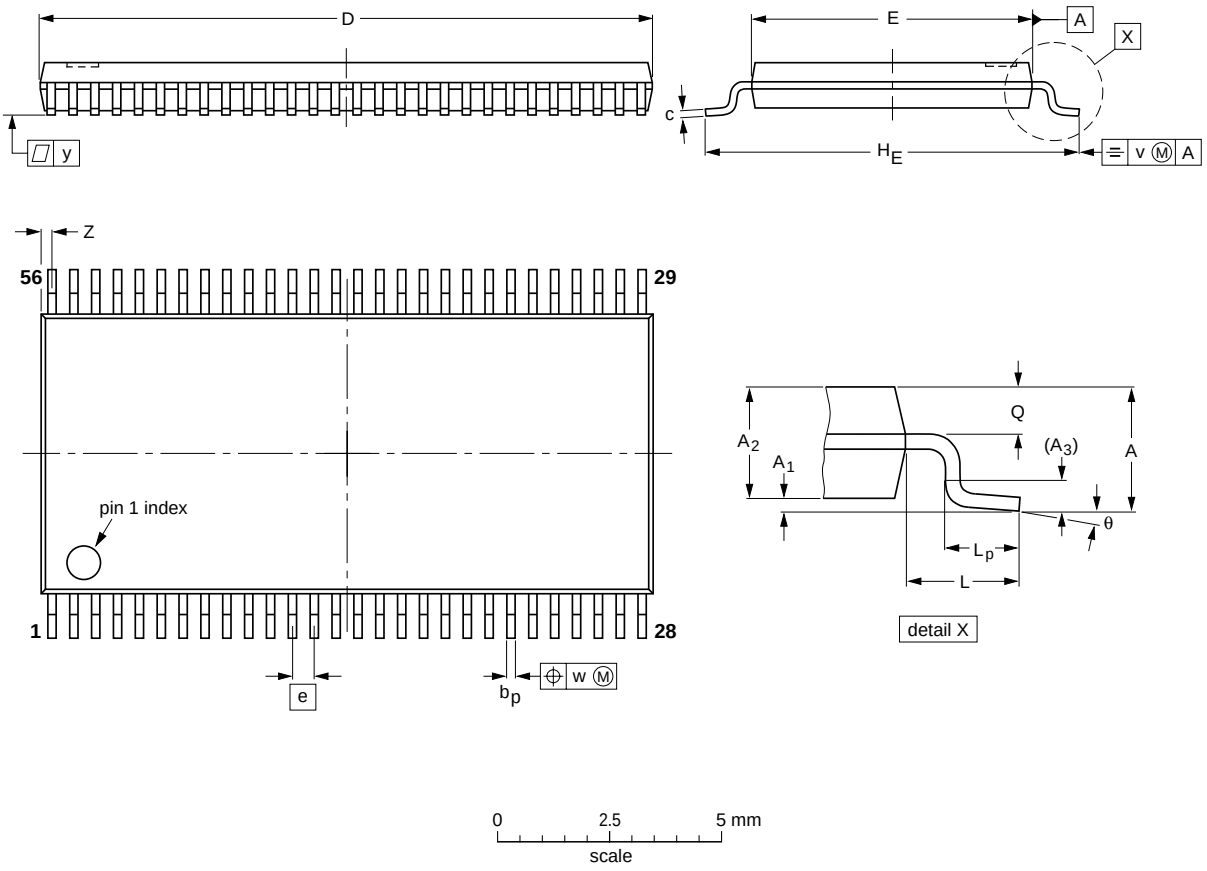
Fig 9. Load circuitry for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

13. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT364-1 (TSSOP56)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16952_2	20060427	Product data sheet	-	74ALVCH16952_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • The symbol of pin numbers 15, 16, 17, 19, 20, 21, 23 and 24 is rectified			
74ALVCH16952_1 (9397 750 04563)	19980901	Preliminary specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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