MAC16CMG, MAC16CNG

Triacs

Silicon Bidirectional Thyristors

Designed primarily for full wave ac control applications, such as motor controls, heating controls or dimmers; or wherever full−wave, silicon gate−controlled devices are needed.

Features

- High Commutating di/dt and High Immunity to dV/dt @ 125°C
- Minimizes Snubber Networks for Protection
- Blocking Voltage to 800 Volts
- On−State Current Rating of 16 Amperes RMS
- High Surge Current Capability − 150 Amperes
- Industry Standard TO−220 Package for Ease of Design
- Glass Passivated Junctions for Reliability and Uniformity
- Operational in Three Quadrants, Q1, Q2, and Q3
- These Devices are Pb−Free and are RoHS Compliant*

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (T_J = −40 to 125°C) MAC16CM / MAC16CN	V_{DRM}, V_{RRM}	600 / 800	V
On-State RMS Current (Full Cycle Sine Wave 50 to 60 Hz; T_C = 80°C)	$I_{T(RMS)}$	16	A
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = 125°C)	I_{TSM}	150	A
Circuit Fusing Consideration (t = 8.33 ms)	I^2t	93	A^2sec
Peak Gate Power (Pulse Width ≤ 1.0 μs, T_C = 80°C)	P_{GM}	20	W
Average Gate Power (t = 8.3 ms, T_C = 80°C)	$P_{G(AV)}$	0.5	W
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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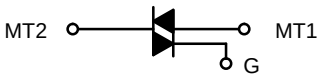
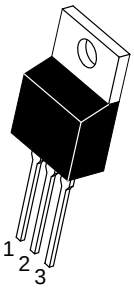
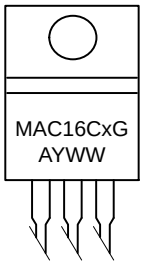
TRIACS
16 AMPERES RMS
400 thru 800 VOLTS



MARKING DIAGRAM



TO−220
CASE 221A
STYLE 4



x = M or N
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

PIN ASSIGNMENT	
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

Device	Package	Shipping
MAC16CMG	TO−220 (Pb−Free)	50 Units / Rail
MAC16CNG	TO−220 (Pb−Free)	50 Units / Rail

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Thermal Resistance,	Junction−to−Case Junction−to−Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds		T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; Electricals apply in both directions)

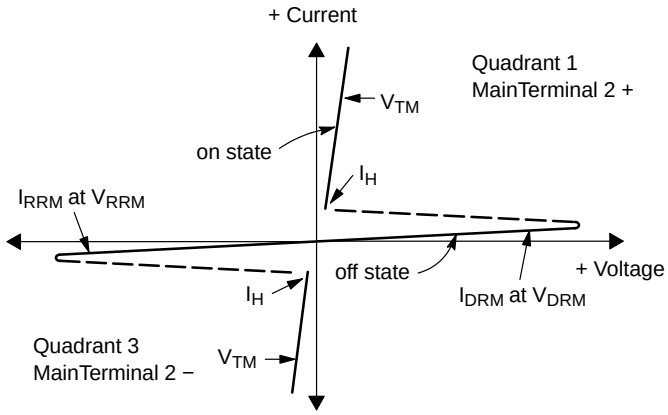
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, V_{RRM} Gate Open)	T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	− −	− −	0.01 2.0	mA
ON CHARACTERISTICS						
Peak On-State Voltage (Note 2) (I_{TM} = ±21 A Peak)		V_{TM}	−	1.2	1.6	V
Gate Trigger Current (Continuous DC) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(−) MT2(−), G(−)		I_{GT}	 8.0 8.0 8.0	 12 16 20	 35 35 35	mA
Holding Current (V_D = 12 V, Gate Open, Initiating Current = ±150 mA)		I_H	−	20	50	mA
Latching Current (V_D = 12 V, I_G = 35 mA) MT2(+), G(+) MT2(+), G(−) MT2(−), G(−)		I_L	 − − −	 25 40 24	 50 80 50	mA
Gate Trigger Voltage (Continuous DC) (V_D = 12 V, R_L = 100 Ω) MT2(+), G(+) MT2(+), G(−) MT2(−), G(−)		V_{GT}	 0.5 0.5 0.5	 0.75 0.72 0.82	 1.5 1.5 1.5	V
DYNAMIC CHARACTERISTICS						
Rate of Change of Commutating Current (V_D = 400 V, I_{TM} = 6.0 A, Commutating dV/dt = 24 V/μs, Gate Open, T_J = 125°C, f = 250 Hz, C_L = 10 μF, L_L = 40 mH, with Snubber)		$(di/dt)_c$	15	−	−	A/ms
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, Gate Open, T_J = 125°C)		dV/dt	600	−	−	V/μs
Repetitive Critical Rate of Rise of On-State Current IPK = 50 A; PW = 40 μsec; diG/dt = 200 mA/μsec; f = 60 Hz		di/dt	−	−	10	A/μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

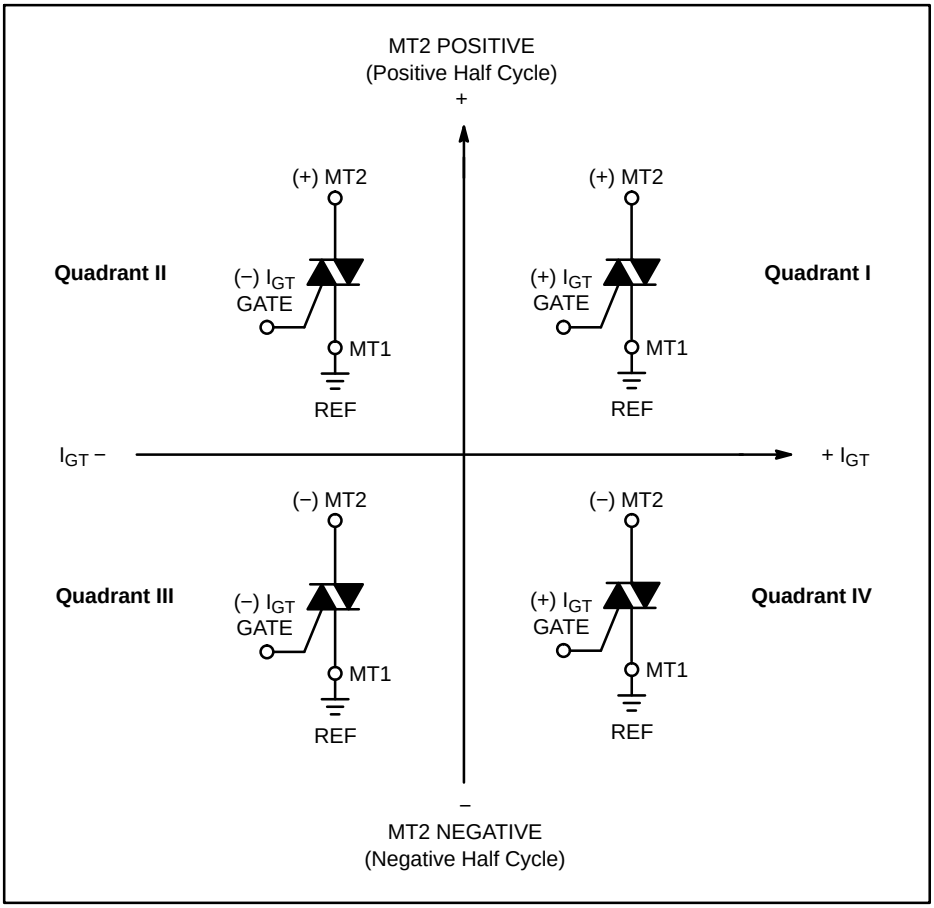
2. Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in−phase signals (using standard AC lines) quadrants I and III are used.

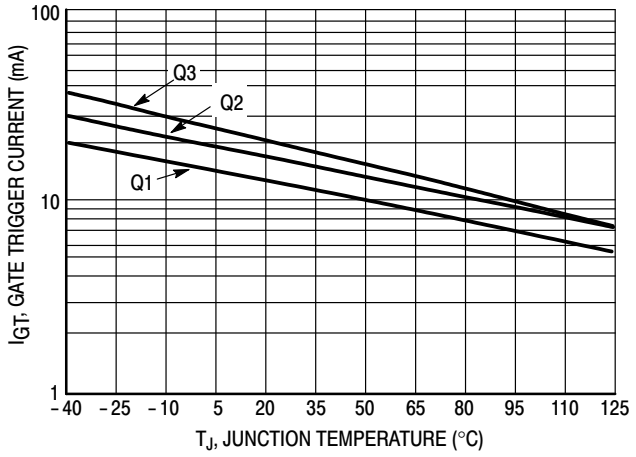


Figure 1. Typical Gate Trigger Current versus Junction Temperature

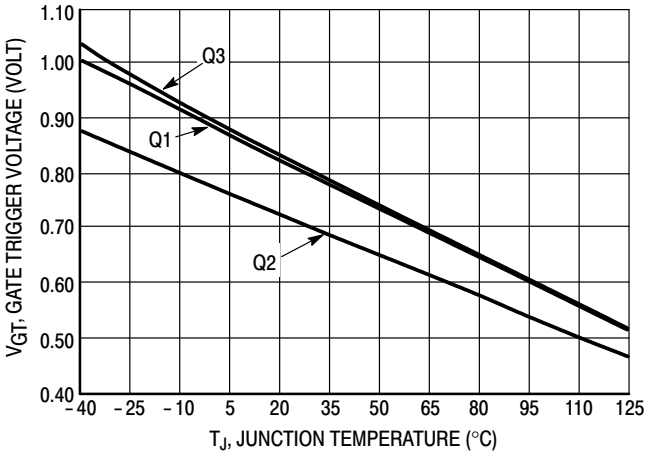


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

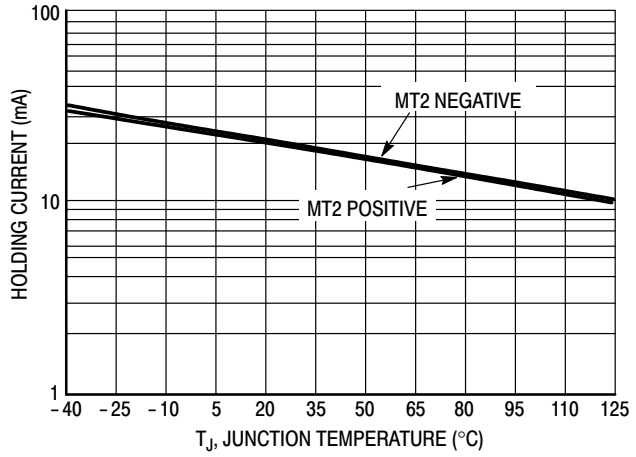


Figure 3. Typical Holding Current versus Junction Temperature

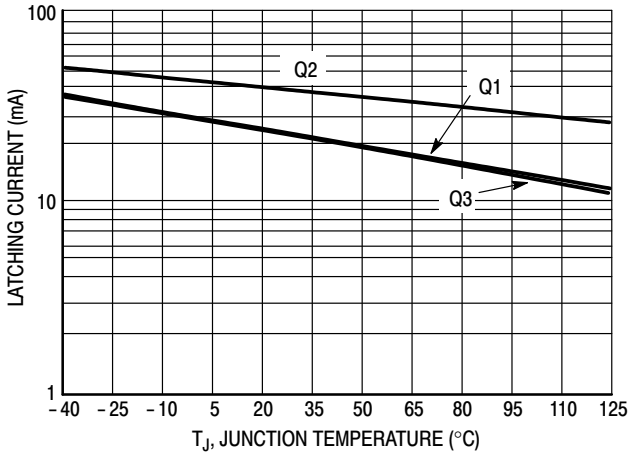


Figure 4. Typical Latching Current versus Junction Temperature

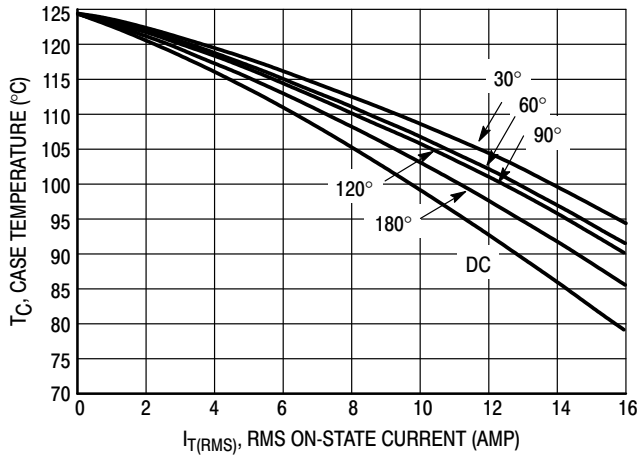


Figure 5. Typical RMS Current Derating

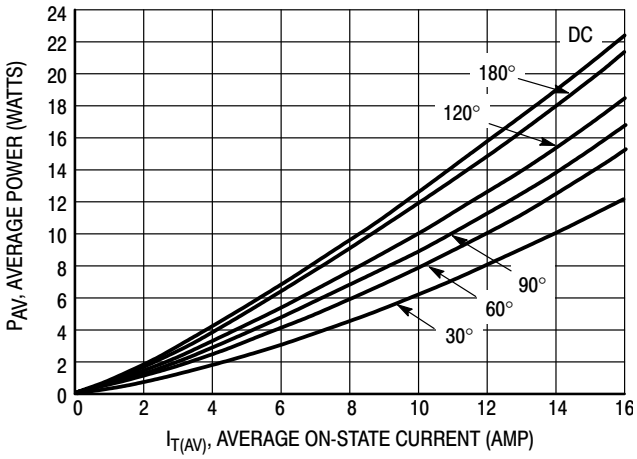


Figure 6. On-State Power Dissipation

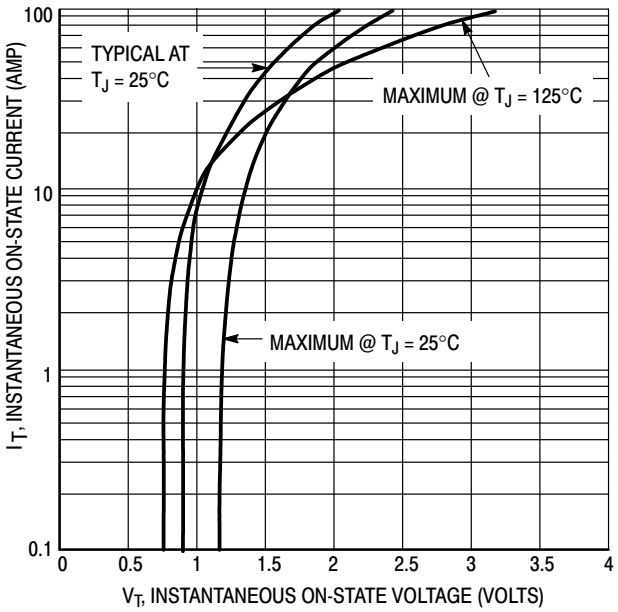


Figure 7. On-State Characteristics

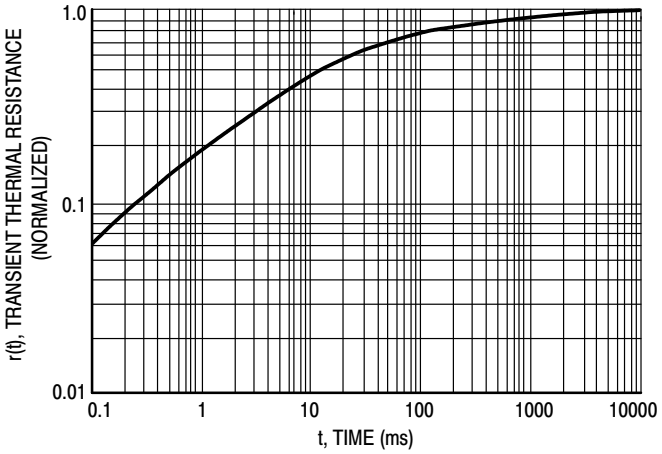
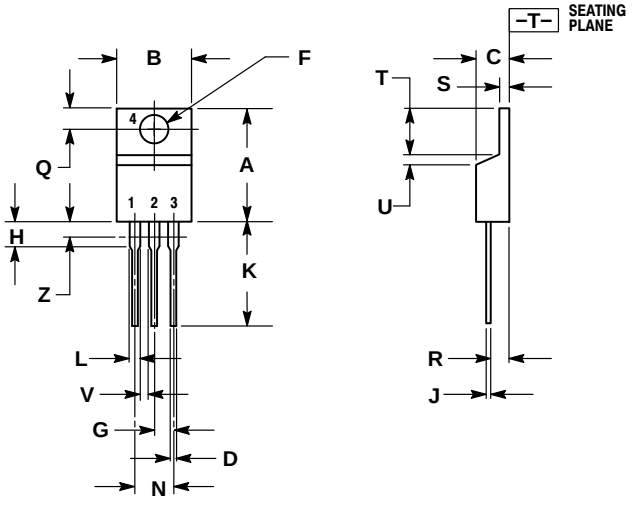


Figure 8. Typical Thermal Response

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

PUBLICATION ORDERING INFORMATION

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