# Microsemi
**INTEGRATED PRODUCTS**

**High Efficiency High Voltage Boost Controller**

**PRODUCTION DATA SHEET**

## DESCRIPTION

The LX1741 is a compact high efficiency step-up boost controller. Featuring a pseudo-hysteretic pulse frequency modulation topology, the LX1741 was designed for maximum efficiency, reduced board size, and minimal cost.

Utilizing an external N-Channel MOSFET, the LX1741 offers designers maximum flexibility with respect to efficiency and cost. The LX1741 provides several design enhancements that improve overall performance under very light load currents by implementing control circuitry that is optimized for portable systems - thus providing a quiescent supply current of only 80μA (typ) and a shutdown current of less than 1μA.

The input voltage ranges from 1.6V to 6.0V, allowing for a wide selection of system battery voltages. Start-up operation is guaranteed at 1.6V input

The output voltage is programmed easily using two external resistors in conjunction with the feedback pin. Depending on the MOSFET selected, the LX1741 is capable of achieving output voltages much higher than 40V.

The LX1741 has an additional feature for simple dynamic adjustment of the output voltage (i.e., up to ±15% of the nominal output voltage). Voltage adjustment is achieved via an analog reference signal or a direct PWM input signal applied to the ADJ pin. Any PWM amplitude is easily accommodated with a single external resistor.

The LX1741 is available in both the 8-Pin MSOP, and the miniature 8-Pin MLP requiring minimal PCB area.

**IMPORTANT:** For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

## KEY FEATURES

- > 85% Maximum Efficiency
- 80μA Typical Quiescent Supply Current
- Externally Programmable Peak Inductor Current Limit For Maximum Efficiency
- Logic Controlled Shutdown
- < 0.5 µA Shutdown Current (typ)
- Dynamic Output Voltage Adjustment Via Analog Reference Or Direct PWM Input
- 8-Pin MSOP Package or 8-Pin MLP

## APPLICATIONS/BENEFITS

- Pagers
- Wireless Phones
- PDAs
- Handheld Computers
- General LCD Bias Applications
- LED Driver

## PRODUCT HIGHLIGHT
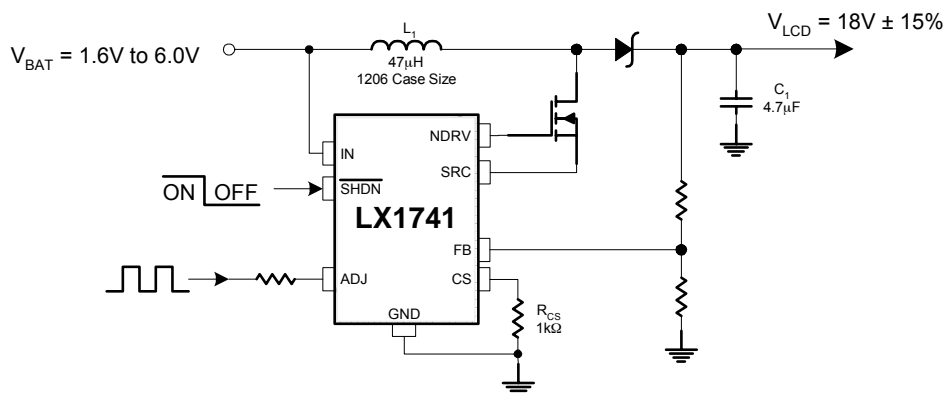


## PACKAGE ORDER INFO

| $T_A$ (°C) | **LM** Plastic MLP 8-Pin | **DU** Plastic MSOP 8-Pin |
|---|---|---|
| | RoHS Compliant / Pb-free Transition DC: 0452 | RoHS Compliant / Pb-free Transition DC: 0432 |
| 0 to 70 | **LX1741CLM** | **LX1741CDU** |

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1741CDU-TR)

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## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{CC}$) .................................................................. -0.3V to 7.0V
Feedback Input Voltage ($V_{FB}$) ............................................. -0.3V to $V_{IN}$ + 0.3V
Shutdown Input Voltage ($V_{\overline{SHDN}}$) ..................................... -0.3V to $V_{IN}$ + 0.3V
PWM Input Amplitude .................................................. -0.3V to $V_{IN}$ + 0.3V
Analog Adjust Input Voltage ($V_{ADJ}$) ................................................ -0.3V to $V_{IN}$
Source Input Current ($I_{SRC}$) ............................................................. 0.80 $A_{RMS}$
Operating Junction Temperature ............................................................. 150°C
Storage Temperature Range ...................................................... -65°C to 150°C
Lead Temperature (Soldering 180 seconds) ............................................ 235°C
Peak Package Solder Reflow Temp. (40 seconds max. exposure) ............... 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

## PACKAGE PIN OUT

SRC — 1 | 8 — NDRV
GND — 2 | 7 — IN
CS — 3 | 6 — FB
ADJ — 4 | 5 — SHDN

**DU PACKAGE**
(Top View)

SRC — 1 | 8 — NDRV
GND — 2 | 7 — IN
CS — 3 | 6 — FB
ADJ — 4 | 5 — $\overline{SHDN}$
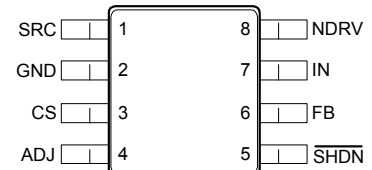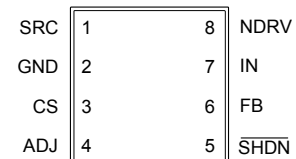
**LM PACKAGE**
(Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish

## THERMAL DATA

**DU** **Plastic MSOP 8-Pin**

| THERMAL RESISTANCE-JUNCTION TO AMBIENT, $\theta_{JA}$ | **206°C/W** |
|---|---|
| THERMAL RESISTANCE-JUNCTION TO CASE, $\theta_{JC}$ | **39°C/W** |

**LM** **Plastic MLP 8-Pin**

| THERMAL RESISTANCE-JUNCTION TO AMBIENT, $\theta_{JA}$ | **41°C/W** |
|---|---|
| THERMAL RESISTANCE-JUNCTION TO CASE, $\theta_{JC}$ | **5.2°C/W** |

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JC})$.
The $\theta_{JA}$ numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

## FUNCTIONAL PIN DESCRIPTION

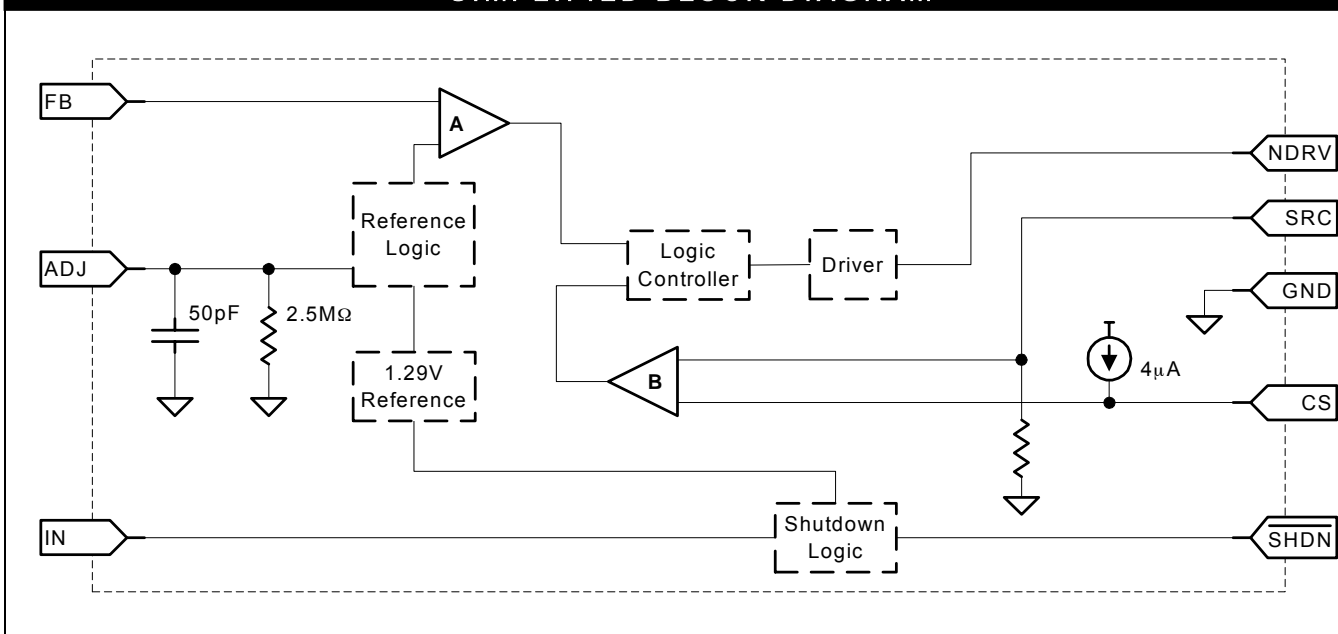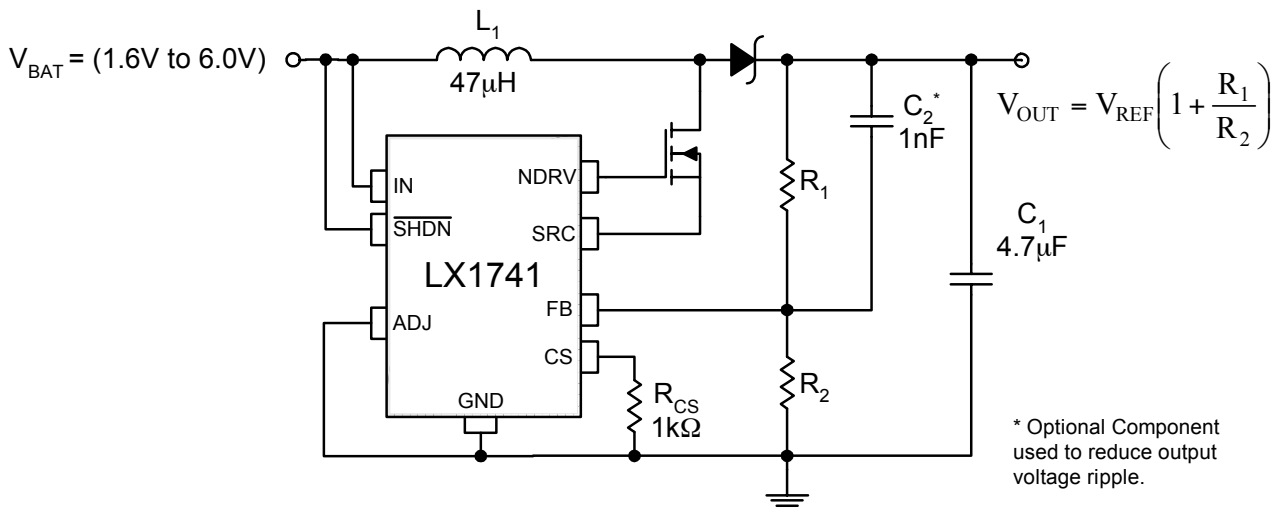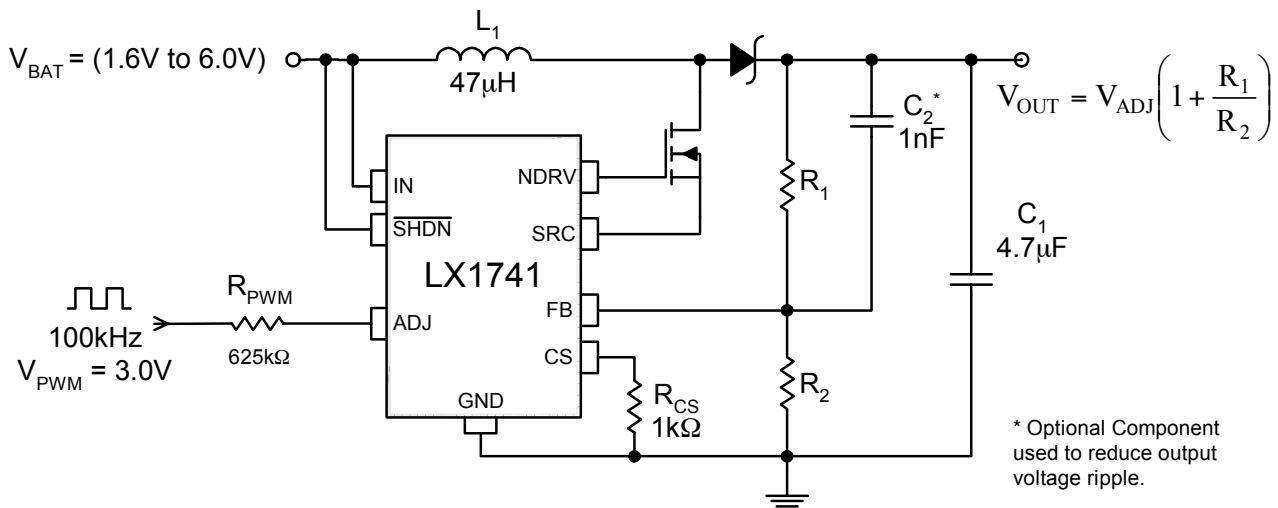| NAME | DESCRIPTION |
|---|---|
| IN | Unregulated IC Supply Voltage Input – Input range from +1.6V to 6.0V. Bypass with a 1μF or greater capacitor for operation below 2.0V. |
| FB | Feedback Input – Connect to a resistive divider network between the output and GND to set the voltage at $V_{FB}$ (see Output Voltage Programming: Application Information). |
| $\overline{SHDN}$ | Active-Low Shutdown Input – A logic low shuts down the device and reduces the supply current to 0.1μA. Connect $\overline{SHDN}$ to $V_{CC}$ for normal operation. |
| NDRV | MOSFET Gate Driver – Connects to an external N-Channel MOSFET. |
| CS | Current-Sense Amplifier Input – Connecting a resistor between CS and GND sets the peak inductor current limit. |
| GND | Common terminal for ground reference. |
| ADJ | An applied PWM Signal Input becomes the internal reference, via an internal filter and gain resistor, thus allowing for a dynamic output voltage adjustment of ±15% (i.e., corresponding to the duty cycle variance). Connecting this pin to ground causes the device to revert to the internal voltage reference (note: refer to figure 8). |
| SRC | MOSFET Current Sense Input - Connects to the External N-Channel MOSFET Source. |

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## ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature $0°C \le T_A \le 70°C$ except where otherwise noted and the following test conditions: $V_{IN}$ = 3V, $V_{OUT}$ = 18.5V, $V_{ADJ}$ = 0V, $R_{LOAD}$ = 9.25k$\Omega$, $\overline{SHDN}$ = $V_{IN}$

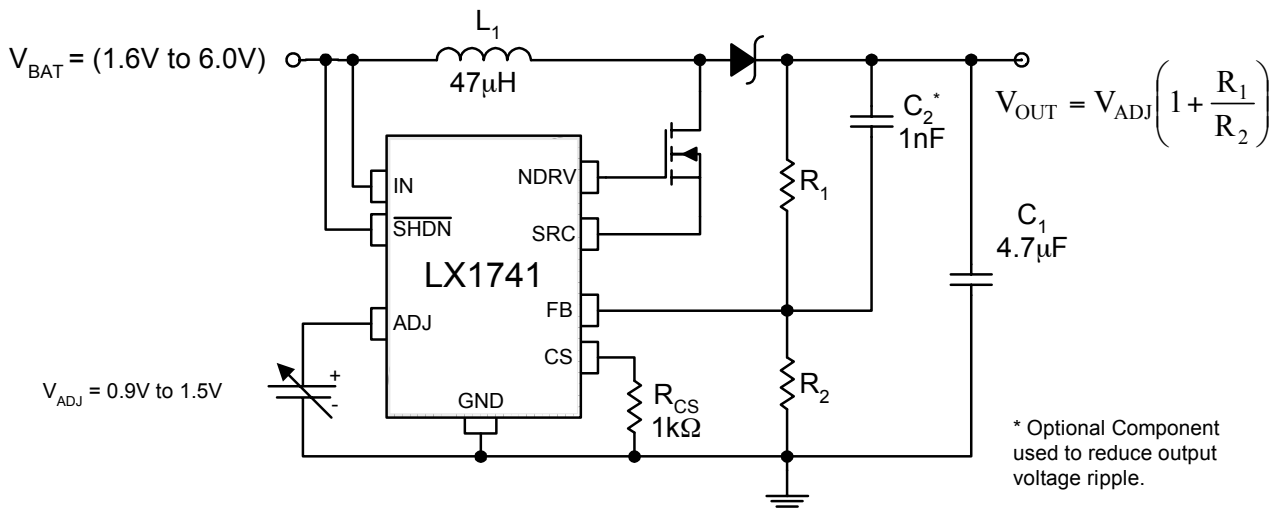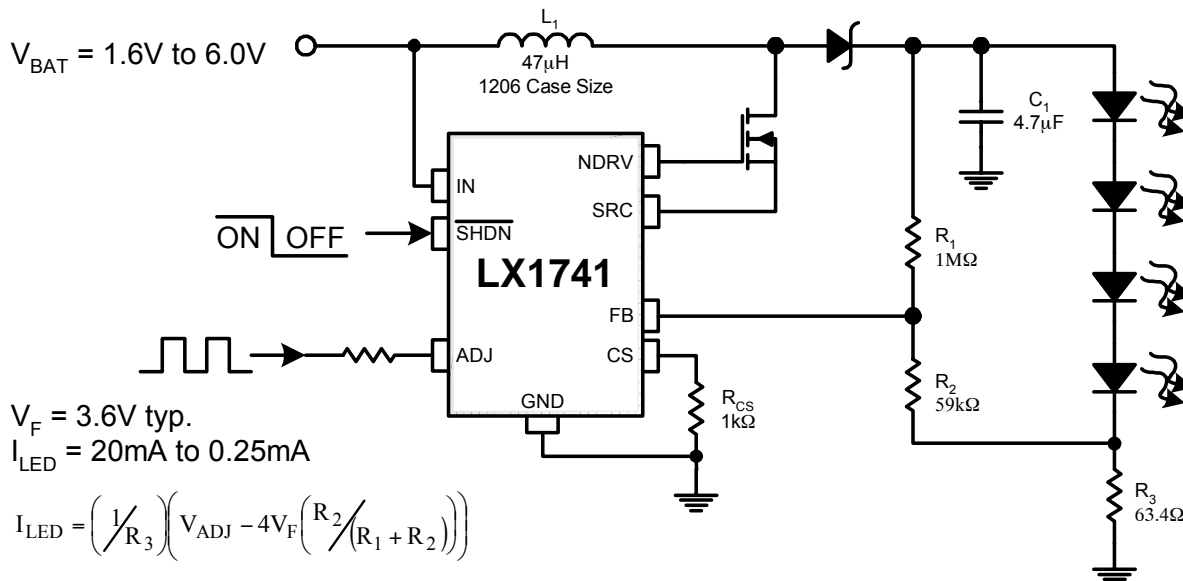| Parameter | Symbol | Test Conditions | LX1741 Min | LX1741 Typ | LX1741 Max | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{IN}$ | | 1.6 | | 6.0 | V |
| Minimum Start-up Voltage | $V_{SU}$ | $T_A$ = +25°C | | | 1.6 | V |
| Start-up Voltage Temperature Coefficient | $k_{VST}$ | | | -2 | | mV/°C |
| Quiescent Current | $I_Q$ | $V_{FB}$ = 1.5V | | 80 | 100 | $\mu$A |
| | | $V_{\overline{SHDN}}$ < 0.4V | | 0.2 | 0.5 | $\mu$A |
| FB Threshold Voltage | $V_{FB}$ | $V_{ADJ}$ = GND | 1.264 | 1.290 | 1.316 | V |
| FB Input Bias Current | $I_{FB}$ | $V_{FB}$ = 1.4V | -200 | | 200 | nA |
| ADJ Input Voltage Range [1] | $V_{ADJ}$ | | 0 | | $V_{IN}$ – 100mV | V |
| ADJ Input Bias Current | $I_{ADJ}$ | $V_{ADJ}$ = $V_{FB}$ = 1.29V | 0.3 | | 1.0 | $\mu$A |
| SRC Input Current | $I_{SRC}$ | | | | 0.8 | $A_{RMS}$ |
| Shutdown Input Bias Current | $I_{\overline{SHDN}}$ | $\overline{SHDN}$ = GND | -50 | | 50 | nA |
| Shutdown High Input Voltage | $V_{\overline{SHDN}}$ | $V_{IN}$ = 2V | 1.6 | | | V |
| Shutdown Low Input Voltage | $V_{\overline{SHDN}}$ | $V_{IN}$ = 2V | | | 0.4 | V |
| Current Sense Bias Current | $I_{CS}$ | | 3.0 | 5.0 | 7.0 | $\mu$A |
| Minimum Peak Current | $I_{MIN}$ | GBNT [2] | | 145 | | mA |
| Comparator A Delay | $t_D$ | GBNT [2] | | 620 | | ns |
| NDRV Sink Current | $I_{SNK}$ | $V_{IN}$ = 5V | 50 | | | mA |
| NDRV Source Current | $I_{SRC}$ | $V_{IN}$ = 5V | 100 | | | mA |
| Minimum Off-Time | $t_{OFF}$ | $V_{FB}$ = 1V | 100 | | 500 | ns |

Notes:
1. When using a DC source to adjust $V_{OUT}$, the recommended $V_{ADJ}$ (range) is from 0.9V to 1.50V: see figure 3 and 8.
2. Guaranteed typical value (not tested) @ $T_A$ = 25°C (see section "Inductor Selection and Current Limit Programming")

## SIMPLIFIED BLOCK DIAGRAM

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**APPLICATION CIRCUITS**

## Typical LCD Bias Applications



$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$$

\* Optional Component used to reduce output voltage ripple.

**Figure 1** – Fixed Output Voltage Operation



$$V_{OUT} = V_{ADJ}\left(1 + \frac{R_1}{R_2}\right)$$

\* Optional Component used to reduce output voltage ripple.

**Figure 2** – Dynamic Output Voltage Operation Via PWM Input

**Note**: An in-series $R_{PWM}$ will attenuate the PWM amplitude to the proper signal level at the ADJ pin. With the $R_{PWM}$ value shown, a PWM signal having a duty of 30% to 50% will generate 0.9V to 1.5V at the ADJ pin.

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## APPLICATION CIRCUITS (CONTINUED)

### Typical LCD Bias Applications (Cont)

$$V_{OUT} = V_{ADJ}\left(1 + \frac{R_1}{R_2}\right)$$

$V_{BAT}$ = (1.6V to 6.0V)

$L_1$ 47μH

$C_2^*$ 1nF

$C_1$ 4.7μF

IN
SHDN
NDRV
SRC
LX1741
ADJ
FB
CS
GND

$V_{ADJ}$ = 0.9V to 1.5V

$R_{CS}$ 1kΩ

$R_1$

$R_2$

\* Optional Component used to reduce output voltage ripple.

**Figure 3** – Dynamic Output Voltage Operation Via Analog Voltage Input

### LED Driver Application

$V_{BAT}$ = 1.6V to 6.0V

$L_1$ 47μH 1206 Case Size

$C_1$ 4.7μF

ON OFF

IN
SHDN
NDRV
SRC
**LX1741**
ADJ
FB
CS
GND

$R_{CS}$ 1kΩ

$R_1$ 1MΩ

$R_2$ 59kΩ

$R_3$ 63.4Ω

$V_F$ = 3.6V typ.
$I_{LED}$ = 20mA to 0.25mA

$$I_{LED} = \left(\frac{1}{R_3}\right)\left(V_{ADJ} - 4V_F\left(\frac{R_2}{R_1 + R_2}\right)\right)$$

**Figure 4** – LED Driver with Full-Range Dimming Via PWM Input

**Note** The component values shown are only examples for a working system. Actual values will vary greatly depending on desired parameters, efficiency, and layout constraints.

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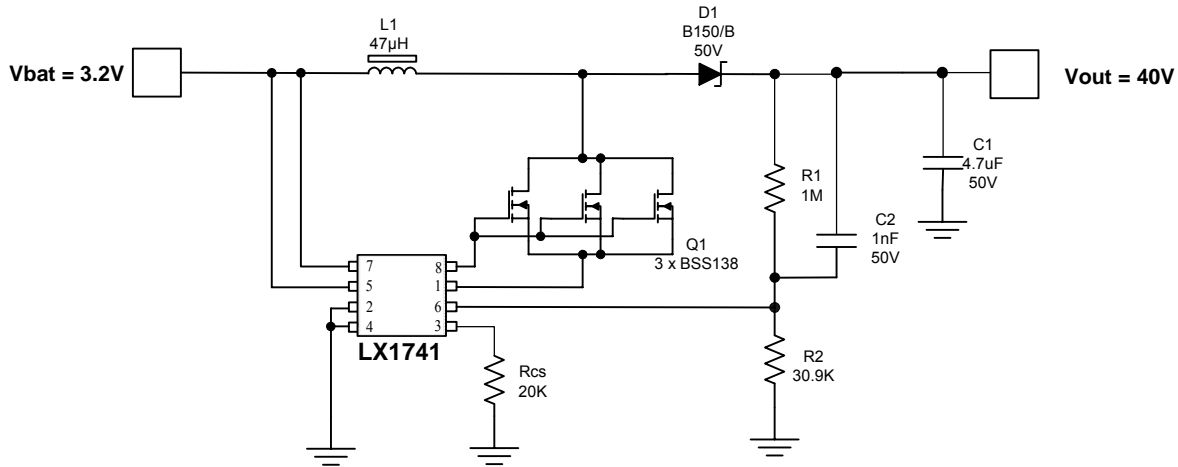
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**APPLICATION CIRCUITS (CONTINUED)**



**Figure 5** – Application of Fixed Output, 40V @ 20mA
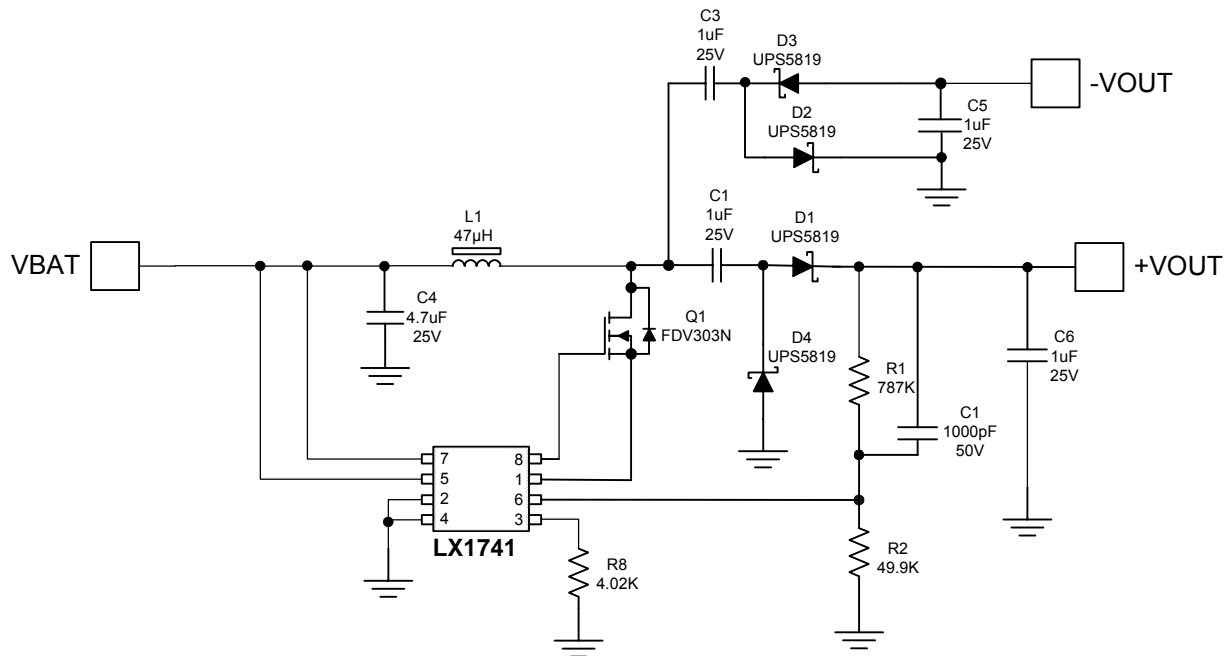


**Figure 6** – Application of Dual Output, ± 20V @ 2mA

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## APPLICATION INFORMATION

### FUNCTIONAL DESCRIPTION

The LX1741 is a Pulse Frequency Modulated (PFM) boost converter that is optimized for large step up voltage applications like LCD biasing. It operates in a pseudo-hysteretic mode with a fixed switch "off time" of 300ns. Converter switching is enabled when the feedback voltage, $V_{FB}$, falls below the 1.29V reference or VADJ (see Block Diagram). When this occurs, comparator A activates the off-time controller. The off-time controller and the current limiter circuit activate comparator B which toggles the NDRV output circuit. The NDRV output is switched "on" (and remains "on") until the inductor current ramps up to the peak current level. This current level is set via the external $R_{CS}$ resistor and monitored through the CS and SRC inputs.

The load is powered from energy stored in the output capacitor during the inductor charging cycle. Once the peak inductor current value is achieved, the NDRV output is turned off (off-time is typically 300ns) allowing a portion of the energy stored in the inductor to be delivered to the load. This causes the output voltage to continue to rise at the input to the feedback circuit (i.e., comparator A). If the voltage at the FB input is still less than 1.29V at the end of the off-time period, the NDRV output switches the external FET "on" and the inductor charging cycle repeats until $V_{FB}$ is greater than the internal reference. This switching behavior is shown in Figure 9 and 11.

The application of an external voltage source at the ADJ pin allows for output voltage adjustment over a typical range of approximately ±15%. The designer can select one of two possible methods. One option is to vary the reference voltage directly at the ADJ pin by applying a DC voltage from 0.9 to 1.5V. The second option is to connect a PWM logic signal to the ADJ pin (e.g., see Figure 2). The LX1741 includes an internal 50pF capacitor to ground that works with an external resistor to create a low-pass filter (i.e., filter out the AC component of a pulse width modulated input of $f_{PWM} \geq 100KHz$).

The adjustment voltage level is selectable (with limited accuracy) by implementing the voltage divider created between the external series resistor and the internal 2.5MΩ resistor. If the DC voltage at the ADJ pin drops below 0.6V, the device will revert to the internal reference voltage level of 1.29V. A typical adjustment curve is shown in Figure 8 (see section titled: Characteristic Curves). Disabling the LX1741 is achieved by driving the SHDN pin with a low-level logic signal thus reducing the device power consumption to less than 1µA.

### OUTPUT VOLTAGE PROGRAMMING

Selecting the appropriate values for R1 and R2 in the voltage divider connected to the feedback pin programs the output voltage. Using a value of 49.9K for R2 works well in most applications. R1 can be determined by the following equation (where $V_{REF} = 1.29V$ nominal):

$$R1 = R2 \times \frac{(V_{OUT} - V_{REF})}{V_{REF}}$$

DESIGN EXAMPLE:

Let R2 equals 49.9K and the required VOUT equal to 18V.

$$R1 = 49.9K\Omega \times \frac{(18V - 1.29V)}{1.29V} = 646.4K\Omega$$

### INDUCTOR SELECTION AND CURRENT LIMIT PROGRAMMING

Setting the level of peak inductor current to, at least, 1.5x the expected maximum DC input current will minimize the inductor size, the input ripple current, and the output ripple voltage. The designer is encouraged to use inductors that will not saturate at the peak inductor current level. An inductor value of 47µH is recommended. Choosing a lower value emphasizes peak current overshoot while choosing a higher value emphasizes output ripple voltage. The peak switch current is defined using a resistor placed between the CS terminal and ground and the $I_{PEAK}$ equation is:

$$I_{PEAK} = I_{MIN} + \left(\frac{V_{IN}}{L}\right)t_D + \left(I_{SCALE}\right)R_{CS}$$

The maximum $I_{PEAK}$ value is limited by the $I_{SRC}$ value (max. = 0.8$A_{RMS}$). The minimum $I_{PEAK}$ value is defined when $R_{CS}$ is zero. A typical value for the minimum peak current ($I_{MIN}$) at 25°C is 145mA. The parameter $t_D$ is related to internal operation of comparator A. A typical value at 25°C is 620ns. A typical value of $I_{SCALE}$ at 25°C is 31mA per KΩ. All of these parameters have an effect on the final $I_{PEAK}$ value.

DESIGN EXAMPLE:

Determine $I_{PEAK}$ where $V_{IN}$ equals 3.0V and $R_{CS}$ equals 4.02KΩ using nominal values for all other parameters.

$$I_{PEAK} = 145mA + \left(\frac{3.0V}{47\mu H}\right) \times 620ns + \left(\frac{31mA}{k\Omega}\right) \times 4.02K\Omega$$

The result of this example yields a nominal $I_{PEAK}$ equal to 145mA + 39.6mA + 124.6ma = 309.2mA.

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## APPLICATION INFORMATION (CONTINUED)

### OUTPUT RIPPLE CAPACITOR SELECTION

Output voltage ripple is a function of the inductor value (L), the output capacitor value ($C_{OUT}$), the peak switch current setting ($I_{PEAK}$), the load current ($I_{OUT}$), the input voltage ($V_{IN}$) and the output voltage ($V_{OUT}$) for a this boost converter regulation scheme. When the switch is first turned on, the peak-to-peak voltage ripple is a function of the output droop (as the inductor current charges to $I_{PEAK}$), the feedback transition error (i.e., typically 10mV), and the output overshoot (when the stored energy in the inductor is delivered to the load at the end of the charging cycle). Therefore the total ripple voltage is

$$V_{RIPPLE} = \Delta V_{DROOP} + \Delta V_{OVERSHOOT} + 10mV$$

The initial droop can be estimated as follows where the 0.5v value in the denominator is an estimate of the voltage drop across the inductor and the FET's $R_{DS\_ON}$:

$$\Delta V_{DROOP} = \frac{\left(\dfrac{L}{C_{OUT}}\right) \times \left(I_{PK} \times I_{OUT}\right)}{\left(V_{IN} - 0.5\right)}$$

The output overshoot can be estimated as follows where the 0.5 value in the denominator is an estimate of the voltage drop across the diode:

$$\Delta V_{OVERSHOOT} = \frac{\frac{1}{2} \times \left(\dfrac{L}{C_{OUT}}\right) \times \left(I_{PK} - I_{OUT}\right)^2}{\left(V_{OUT} + 0.5 - V_{IN}\right)}$$

DESIGN EXAMPLE:

Determine the $V_{RIPPLE}$ where $I_{PK}$ equals 200mA, $I_{OUT}$ equals 35mA, L equals 47µH, $C_{OUT}$ equals 4.7µF, $V_{IN}$ equals 3.0V, and $V_{OUT}$ equals 18.0V:

$$\Delta V_{DROOP} = \frac{\left(\dfrac{47µH}{4.7µF}\right) \times \left(200mA \times 35mA\right)}{\left(3.0 - 0.5\right)} = 28mV$$

$$\Delta V_{OVERSHOOT} = \frac{\frac{1}{2} \times \left(\dfrac{47µH}{4.7µF}\right) \times \left(200mA - 35mA\right)^2}{\left(18.0 + 0.5 - 3.0\right)} = 9.4mV$$

Therefore, for $C_{OUT}$ equals 4.7µF:

$$V_{RIPPLE} = 28mV + 9.4mV + 10mV = 47.4mV$$

Increasing the output capacitor value results in the reduction of the output voltage ripple voltage. Low ESR capacitors are recommended to reduce ripple caused by the switching current. Multi-layer ceramic capacitors with X5R or X7R dielectric are a superior choice featuring small size, very low ESR, and a temperature stable dielectric. Low ESR electrolytic capacitors such as solid tantalum or OS-CON types are also acceptable. Moreover, adding a capacitor from the output to the feedback pin (C2) allows the internal feedback circuitry to respond faster which further minimizes output voltage ripple and reduces noise coupling into the high impedance feedback input.

### DIODE SELECTION

A Schottky diode is recommended for most applications (e.g. Microsemi UPS5819). The low forward voltage drop and fast recovery time associated with this device supports the switching demands associated with this circuit topology. The designer is encouraged to consider the diode's average and peak current ratings with respect to the application's output and peak inductor current requirements. Further, the diode's reverse breakdown voltage characteristic must be capable of withstanding a negative voltage transition that is greater than $V_{OUT}$.

### TRANSISTOR SELECTION

The LX1741 can drive up to 100mA of gate drive current. An N-channel MOSFET with a relatively low threshold voltage, low gate charge and low $R_{DS(ON)}$ is required to optimize overall circuit performance. The LXE1741 Evaluation Board uses a Fairchild FDV303. This NMOS device was chosen because it demonstrates an $R_{DS\_ON}$ of 0.33Ω and a total gate charge $Q_g$ of 1.64nC (typ.).

### PCB LAYOUT

The LX1741 produces high slew-rate voltage and current waveforms hence; the designer should take this into consideration when laying out the circuit. Minimizing trace lengths from the IC to the inductor, transistor, diode, input and output capacitors, and feedback connection (i.e., pin 6) are typical considerations. Moreover, the designer should maximize the DC input and output trace widths to accommodate peak current levels associated with this circuit.

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## EVALUATION BOARD

### OVERVIEW

The LXE1741 evaluation board is available from *Microsemi* for assessing overall circuit performance. The evaluation board, shown in Figure 5, is 3 by 3 inches (i.e., 7.6 X 7.6cm) square and factory calibrated to provide a nominal 18V output from a 1.6V to 6.0V input. Circuit designers can easily modify output voltage and current to suit their particular application by replacing the R1 and $R_{CS}$ values respectively. Moreover, inductor, FET, and diodes are easily swapped out to promote design verification of a circuit that maximizes efficiency and minimizes cost for any particular application. The input and output connections are described in Table 1.

### ELECTRICAL CONNECTIONS

Apply the DC input voltage to VBAT (*not VCC*) however, the LX1741 IC may be driven from a separate DC source via the VCC input (if desired). Connect the test load to VOUT. Primary output voltage adjustment is accomplished by selecting the appropriate value for R1. Optional fine adjustment of the output voltage is achieved by applying either a DC voltage or a PWM-type signal to the VADJ input. Both low frequency (f < 100KHz) and high frequency (f > 100KHz) PWM signals are accommodated by choosing the appropriate jumper connection. Further, the VADJ circuit can be bypassed by selecting the appropriate jumper position (see Table 2).

The LX1741 exhibits a low quiescent current ($I_Q$ < 1µA: typ) during shutdown mode. The SHDN pin can be used to examine shutdown performance on the evaluation board. This pin is pulled-up to VCC via a 10KΩ resistor. Grounding the SHDN pin shuts down the IC however, the load is still capable of drawing current through the inductor & diode circuit path. Hence, $V_{OUT}$ during shutdown will be approximately $V_{BAT}$ minus the inductor and diode forward voltage drop.

The LX1741 can achieve output voltages in excess of 25V. In certain applications, it is necessary to protect the load from excessive voltage excursions. The evaluation board provides a VLIM jumper position for this purpose. Engaging this jumper position ensures that the output voltage does not exceed 25V.

The LXE1741 evaluation board provides an easy and cost effective solution for evaluation on the LX1741. The factory installed component list for the evaluation board is provided in Table 3 and the schematic is shown in Figure 6.
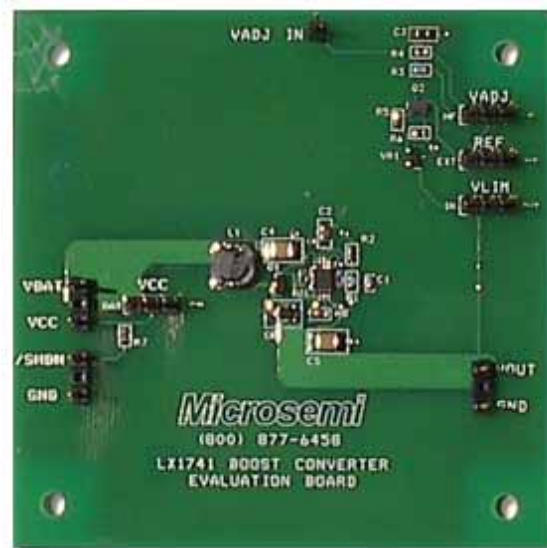


**Figure 7** – LX1741 Circuit Evaluation Board

### Table 1: Input and Output Pin Assignments

| Pin Name | Allowable Range | Description |
|---|---|---|
| VBAT | 0 to 6V | Main power supply for output. (Set external current limit to 0.5A) |
| VCC | 1.6V to 6V | LX1741 power. May be strapped to VBAT or use a separate supply if VCC jumper is in the SEP position. *Do not power output from VCC pin on board..* |
| SHDN | 0 to VCC | Pulled up to VCC on board (10KΩ), Ground to inhibit the LX1741. |
| VOUT | VCC to 25V | Programmed for 18V output, adjustable up to 25V. |
| VADJ IN | 0 to VCC | Apply a DC input or PWM input to adjust the output voltage. |

Note: All pins are referenced to ground.

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**EVAL BOARD**

## EVALUATION BOARD (CONTINUED)

### Table 2: Jumper Pin Position Assignments

| Jumper / Position | Function |
|---|---|
| VCC/ VBAT | Use this position when powering VBAT and VCC from the same supply. Do not connect power to the VCC input when using this jumper position. |
| VCC/ SEP | Use this position when using a separate VCC supply (different from VBAT). |
| REF/ EXT | Use this position when using an external source to adjust the output voltage. |
| REF/ INT | Use this position when using the fixed output voltage mode. In this mode the output voltage can be varied by changing the value of R1 as described in the data sheet. |
| ADJ/ HF | Use this position when adjusting the output with an external PWM that has a repetition rate in excess of 100KHz. |
| ADJ/ LF | Use this position when adjusting the output with an external PWM that has a repetition rate less than 100KHz. Or when using a DC adjustment voltage. |
| VLIM/ IN | Use this position when adjusting the output voltage to prevent the output voltage from accidentally exceeding 25V. |
| VLIM/ OUT | This position disables the output voltage adjustment clamp. This position may be desired if maximizing efficiency when operating near 25V output level. |

Note: Always put jumpers in one of the two possible positions

### Table 3: Factory Installed Component List for the LX1741Evaluation Board

| Ref | Description | Supplier | Part Number |
|---|---|---|---|
| C1 | CAPACITOR, COG, 1000pF, 0402, 50V | MURATA | GRM36X7R102M050 |
| C2 | CAPACITOR, X7R, 0.1uF, 0805, 50V | MURATA | GRM40X7R104M050 |
| C3 | CAPACITOR, Y5V, 2.2uF, 0805, 16V | AVX | 0805YG225ZAT |
| C4,5 | CAPACITOR, X5R, 4.7uF, 1210, 25V | TAIYO YUDEN | CETMK325BJ475MN |
| CR1 | RECTIFIER, SCHOTTKY, 1A, 40V, POWERMITE | MICROSEMI | UPS5819 |
| L1 | INDUCTOR, 47UH, 480mA, SMT | TOKO | A920CY-470M |
| JP1-7 | 3 TERM HEADER, 0.1 IN CTR | 3M | 929647-09-36-I |
| SB1-4 | JUMPER | 3M | 929955-06 |
| Q1 | MOSFET, N-CHAN, 25V, SOT-23 | FAIRCHILD | FDV303N |
| Q2 | TRANSISTOR, NPN, 40V, SOT-23 | ON | MMBT3904LT1 |
| R1 | RESISTOR, 698K, 1/16W, 0603 | PANASONIC | ERJ3EKF6983 |
| R2 | RESISTOR, 49.9K, 1/16W, 0603 | PANASONIC | ERJ3EKF4992 |
| R3 | RESISTOR, 619K, 1/16W, 0603 | PANASONIC | ERJ3EKF6193 |
| R4 | RESISTOR, 100K, 1/16W, 0603 | PANASONIC | ERJ3EKF1003 |
| R5,R6 | RESISTOR, 1.00K, 1/16W, 0603 | PANASONIC | ERJ3EKF1001 |
| R7 | RESISTOR, 10.0K, 1/16W, 0603 | PANASONIC | ERJ3EKF1002 |
| R8 | RESISTOR, 4.02K, 1/16W, 0603 | PANASONIC | ERJ3EKF4021 |
| U1 | IC, BOOST CONTROLLER | MICROSEMI | LX1741 |
| VR1 | ZENER, 24V,225mW, SOT-23 | ON | BZX84C24LT1 |

Note: The minimum part set for a working power supply consists of: C1, C2, C5, CR1, L1, Q1, R1, R2, R8, U1

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**EVAL BOARD**

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## EVALUATION BOARD (CONTINUED)



**Figure 8** – LX1741 Boost Evaluation Board Schematic
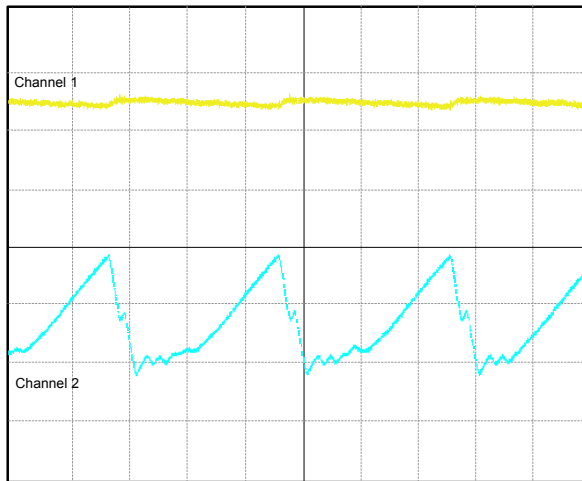
## CHARACTERISTIC CURVES



**Figure 9 –** V$_{OUT}$ and Inductor Current Waveforms
Channel 1: V$_{OUT}$ (AC coupled; 100mV/div)
Channel 2: Inductor Current (100mA/div.)
Configuration: V$_{IN}$ = 1.6V, V$_{OUT}$ = 5.0V, I$_{OUT}$ = 20.0mA



**F**

**igure 10 –** Typical V$_{OUT}$ versus V$_{ADJ}$

- 0 ~ 0.6V : LX1741 uses internal 1.29V reference.
- 0.7V ~ 0.8V : transition from internal to external reference.
- 0.9 to 1.6V : LX1741 defaults to external voltage reference.

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## CHARACTERISTIC CURVES



**Figure 11 –** V$_{OUT}$ and Inductor Current Waveforms (mA)
Channel 1: V$_{OUT}$ (AC coupled; 100mV/div)
Channel 2: Inductor Current (100mA/div.)
Configuration: V$_{IN}$ = 3.0V, V$_{OUT}$ = 17.9V, I$_{OUT}$ = 11.0mA
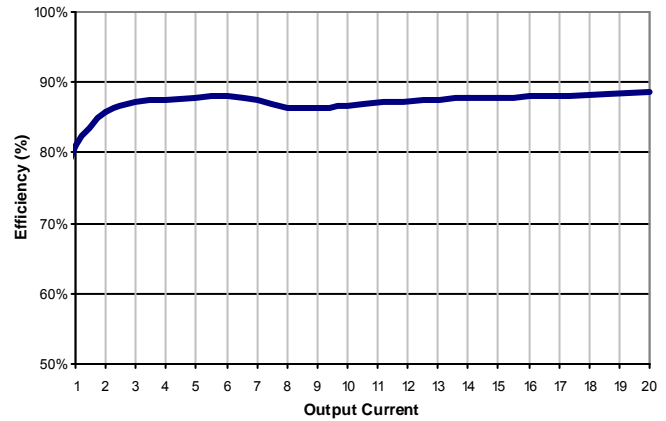


**Figure 12 –** Efficiency vs. Output Current (mA)
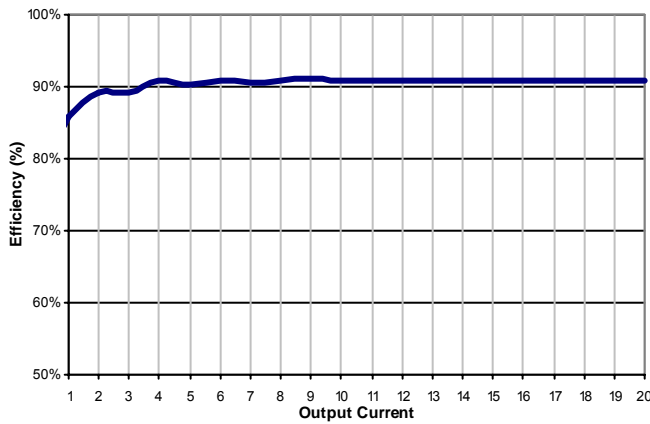Configuration: V$_{IN}$ = 3.0V, V$_{OUT}$ = 17.9V, L1 = 47.0μH



**Figure 13 –** Efficiency vs. Output Current (mA)
Configuration: V$_{IN}$ = 5.2V, V$_{OUT}$ = 17.9V, L1 = 94.0μH
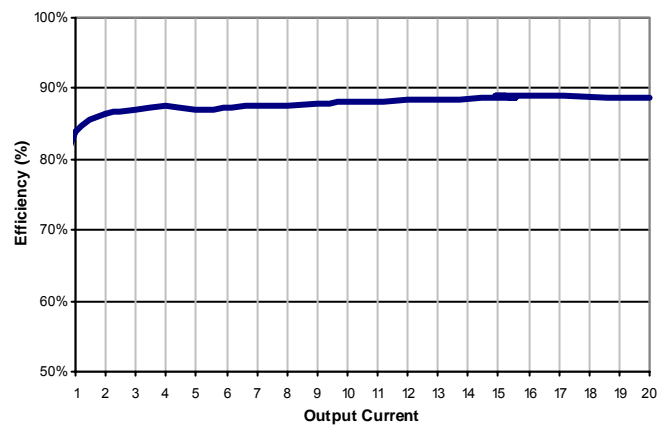


**Figure 14 –** Efficiency vs. Output Current (mA)
Configuration: V$_{IN}$ = 3.0V, V$_{OUT}$ = 10.0V, L1 = 47.0μH

**C**HARTS

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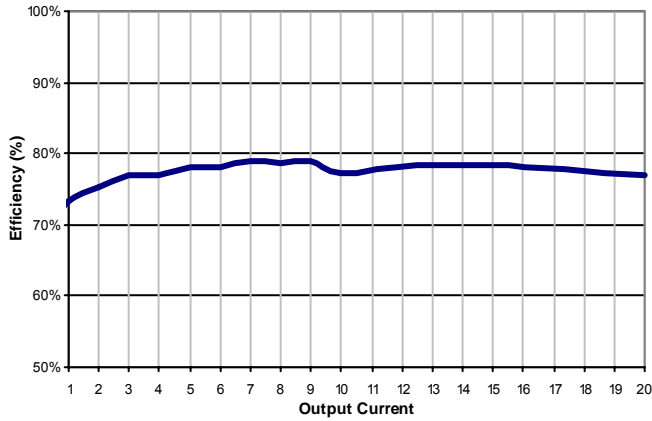
## CHARACTERISTIC CURVES

**Figure 15 –** Efficiency vs. Output Current (mA)
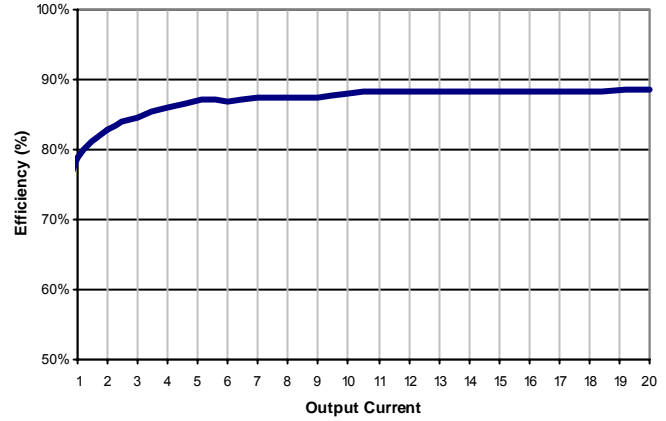Configuration: $V_{IN}$ = 1.6V, $V_{OUT}$ = 5.0V, L1 = 47.0µH

**Figure 16 –** Efficiency vs. Output Current (mA)
Configuration: $V_{IN}$ = 3.0V, $V_{OUT}$ = 5.0V, L1 = 47.0µH

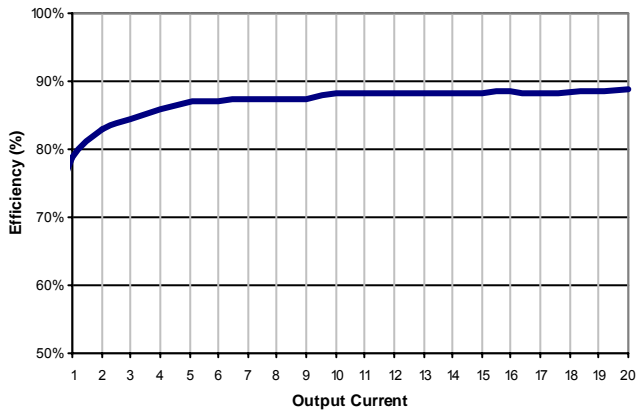**Figure 17 –** Efficiency vs. Output Current (mA)
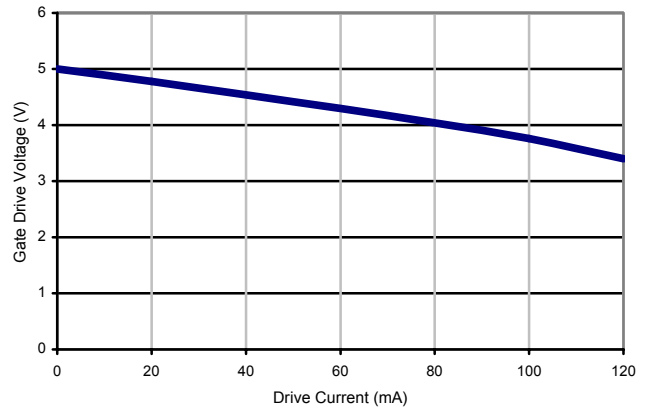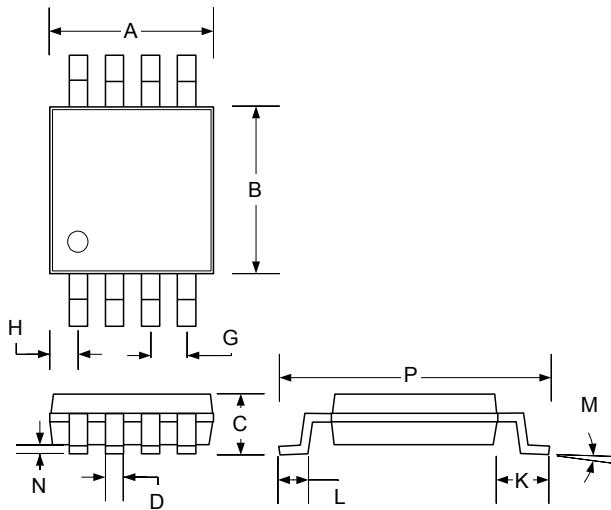Configuration: $V_{IN}$ = 3.0V, $V_{OUT}$ = 5.0V, L1 = 47.0µH

**Figure 18** – Gate Drive Voltage vs. Drive Current (mA)

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**High Efficiency High Voltage Boost Controller**

PRODUCTION DATA SHEET

## PACKAGE DIMENSIONS

### DU  8-Pin Miniature Shrink Outline Package (MSOP)

| Dim | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | **MIN** | **MAX** | **MIN** | **MAX** |
| A | 2.85 | 3.05 | .112 | .120 |
| B | 2.90 | 3.10 | .114 | .122 |
| C | – | 1.10 | – | 0.043 |
| D | 0.25 | 0.40 | 0.009 | 0.160 |
| G | 0.65 BSC | | 0.025 BSC | |
| H | 0.38 | 0.64 | 0.015 | 0.025 |
| J | 0.13 | 0.18 | 0.005 | 0.007 |
| K | 0.95 BSC | | 0.037 BSC | |
| L | 0.40 | 0.70 | 0.016 | 0.027 |
| M | 3° | | 3° | |
| N | 0.05 | 0.15 | 0.002 | 0.006 |
| P | 4.75 | 5.05 | 0.187 | 0.198 |

### LM  8-Pin Plastic MLP-Micro Exposed Pad

Internally Connected together, but isolated from all other terminals
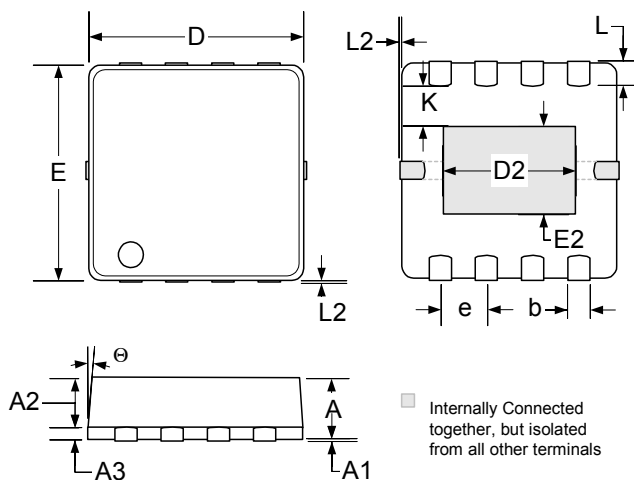
| Dim | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | **MIN** | **MAX** | **MIN** | **MAX** |
| A | 0.80 | 1.00 | 0.031 | 0.039 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| A2 | 0.65 | 0.75 | 0.025 | 0.029 |
| A3 | 0.15 | 0.25 | 0.005 | 0.009 |
| b | 0.28 | 0.38 | 0.011 | 0.015 |
| D | 2.90 | 3.10 | 0.114 | 0.122 |
| E | 2.90 | 3.10 | 0.114 | 0.122 |
| e | 0.65 BSC | | 0.025 BSC | |
| D2 | 1.52 | 2.08 | 0.060 | 0.082 |
| E2 | 1.02 | 1.31 | 0.040 | 0.052 |
| K | 0.20 | * | 0.008 | * |
| L | 0.20 | 0.60 | 0.008 | 0.023 |
| L2 | 0 | 0.13 | 0 | 0.005 |
| Θ | 0° | 12° | 0° | 12° |

**Note:**
1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

MECHANICALS

## NOTES

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